xCORE multicore microcontrollers

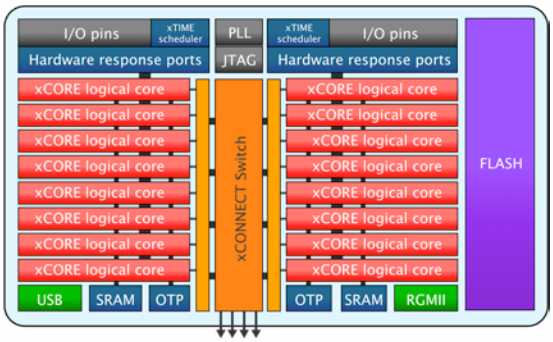
An intelligent approach to embedded processing

For many decades, traditional processor architectures have evolved to fulfil the increasingly demanding requirements of contemporary applications, typically expressed in sequential languages like C. The classical single-core embedded RISC processor has evolved deep pipelines and complex memory and peripheral subsystems. These measures were required to meet demands for increasing performance whilst accommodating the slower bulk memory technologies that are large enough to contain the growing code-bases. The same measures have rendered these architectures ill-equipped to deal with the real-time requirements of their ever-more-complex peripherals.

***xCORE** - designed to respond instantly*

Real-time systems are systems whose functionality depends on performing computations within known deadlines. The need to adhere to such deadlines makes particular demands of the architecture on which a real-time system is implemented. If the architecture itself is not well suited to this type of programming the developer may have to accommodate this in some way, such as over-provisioning (i.e. requiring a much faster processor than is needed on average to meet the worst case), accepting the failure and implementing special "recovery" methods when things go wrong, or even sacrificing flexibility and implementing the most challenging real-time part of the system directly in hardware.

By comparison, the xCORE architecture is a novel approach that divides the application into elements whose disparate demands can be accommodated by dedicated processing cores that form an array. The basic building block is a 32bit RISC processor with dedicated register files and tightly coupled local memory. Processors can communicate with each other through memory or through a network that connects all processors. A hierarchy of interconnect is provided – processors on a tile have direct connection and interfaces between tiles pass through a high-speed switch.



***xCORE-200** XEF216*

The processors are designed to respond instantly to events – either external I/O events, timers or processor events. This allows the xCORE devices to build functions previously requiring hardware – using a processor and software.

In comparison to a traditional processor system, by eliminating all sources of timing uncertainty (operating systems, interrupts caches, busses and other shared resources), xCORE delivers completely predictable performance to the application.