

xCORE-200 Microphone Array Platform Hardware Manual

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xCORE-200 Microphone Array Reference Design is an application specific design targeted at Voice User Interface (VUI) and smart microphone applications. It integrates all the necessary building blocks including: multiple omni-directional microphones, on-board low-jitter clock sources, configurable user input buttons and a 10/100 Mbp/s Ethernet port for connectivity.

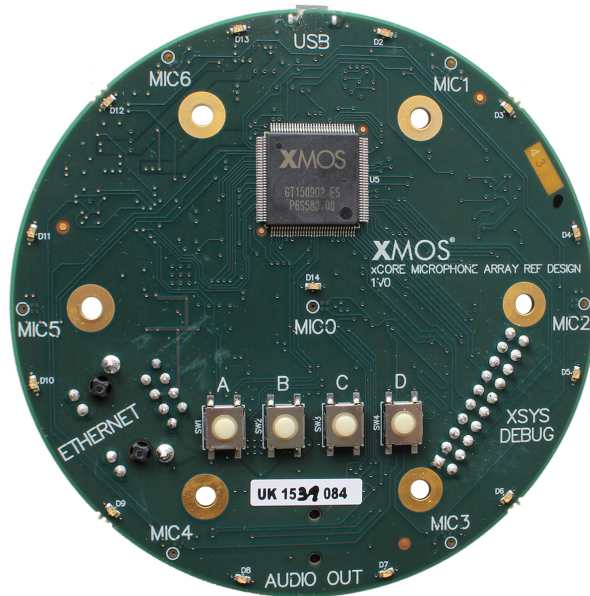


Figure 1:
xCORE-200
Microphone
Array
Reference
Board - top

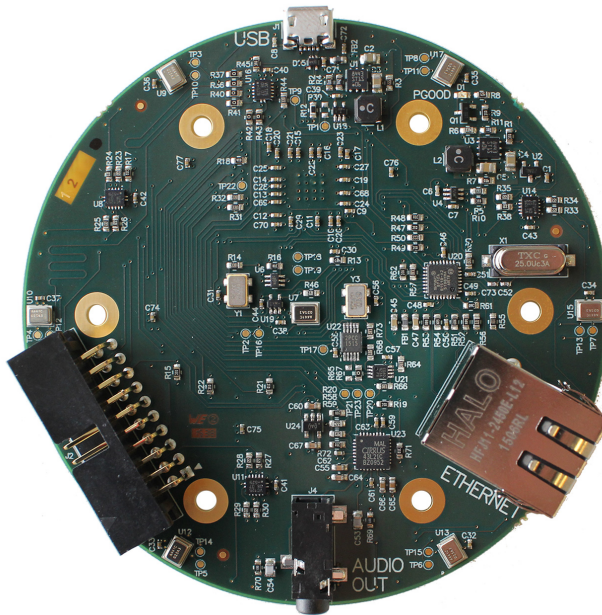


Figure 2:
xCORE-200
Microphone
Array
Reference
Board -
bottom

1 Features

The xCORE-200 Microphone Array Reference Platform block diagram is shown below. It includes:

- ▶ xCORE-200 (XUF216-512-TQ128) Multicore Microcontroller device
- ▶ Seven AKUSTIA AKU441 MEMS Microphones
- ▶ A micro-USB connector
- ▶ An RJ45 connector for 10/100Mbps Ethernet connectivity
- ▶ Four general purpose push-button switches
- ▶ 12 user-controlled LEDs
- ▶ A green 3.3v power-good LED
- ▶ Low-jitter clock source
- ▶ An xSYS connector for an xTAG debug adapter

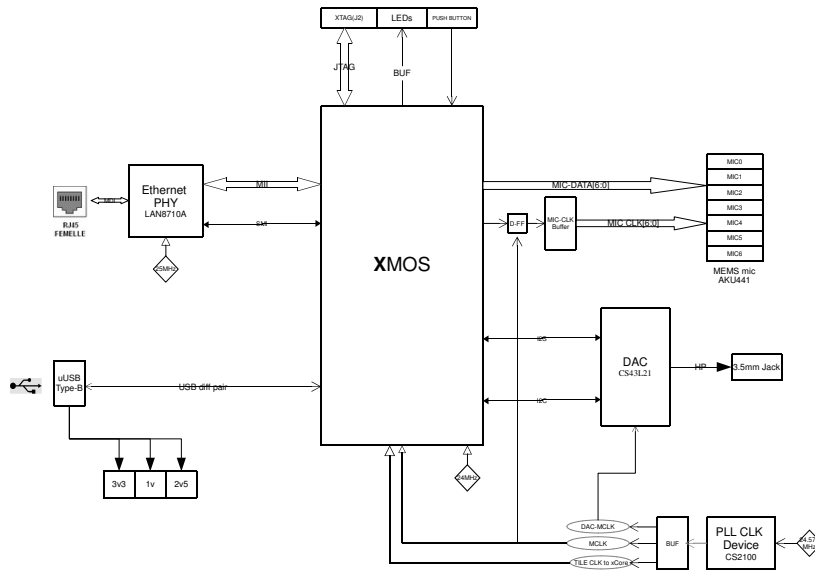


Figure 3:
xCORE-200
Microphone
Array
Reference
Platform
block
diagram

2 Introduction

The xCORE-200 Microphone Array Reference Platform is based on a two-tile xCORE-200 XUF216-512-TQ128 device, which contains 16 32-bit logical processing cores that deliver up to 2000 MIPS compute.

For general information on xCORE-200 devices see the xCORE-200 Architecture Overview¹.

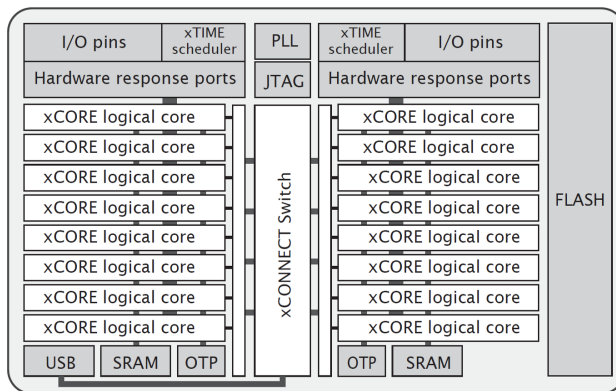


Figure 4:
xCore-200
XUF216-512-
TQ128
device

3 Clock sources and distribution

The board includes four clock sources:

- ▶ xCORE-200 Reference clock - 24MHz oscillator (Y1)
- ▶ Ethernet PHY reference Clock - 25MHz crystal (X1)
- ▶ Low jitter clock source - 24.576MHz oscillator, used as reference clock to Fractional-N clock multiplier (U22)
- ▶ CS2100-CP (CirrusLogic) - Generates a low-jitter output clock that is distributed through buffer NC7NZ34 (U21), and connected to: xCORE-200 device (Tile1 & MCLK), DAC (MIC-CLK).

The CS2100-CP device is configured using I2C interface.

¹<http://www.xmos.com/published/xcore-architecture>

4 Stereo DAC with headphone amplifier

Audio output from the CS43L21 stereo DAC/HPA (U23) is connected to the 3.5mm audio jack (J4) using an I2S interface.

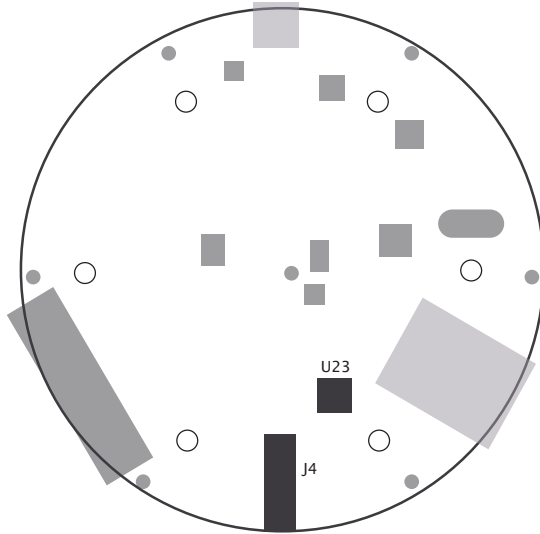


Figure 5:
Stereo
DAC/HPA
components

The CS43L21 stereo DAC/HPA device is configured using the I2C bus.

Pin	Port	Signal
X1D26	P4E0	I2C_SCL
X1D27	P4E1	I2C_SDA
X1D28	P4F0	DAC_RST_N
X1D36	P1M0	I2S_BCLK
X1D37	P1N0	I2S_LRCLK
X1D39	P1P0	I2S_DAC_DATA

The addresses of the CS2100-CP and CS43L21 devices on the I2C bus are shown below.

Device	Ref ID	Address
CS2100-CP	U22	0b1001110 0x4E
CS43L21	U23	0b1001010 0x4A

5 MEMS Microphones

The AKU441 MEMS microphones used in this reference platform have a bottom port and measure 4mmx3mmx1 mm, suitable for voice interface applications.

One microphone is placed at the center of the board (MIC_0). The remaining six microphones are distributed equidistant around the board edge.

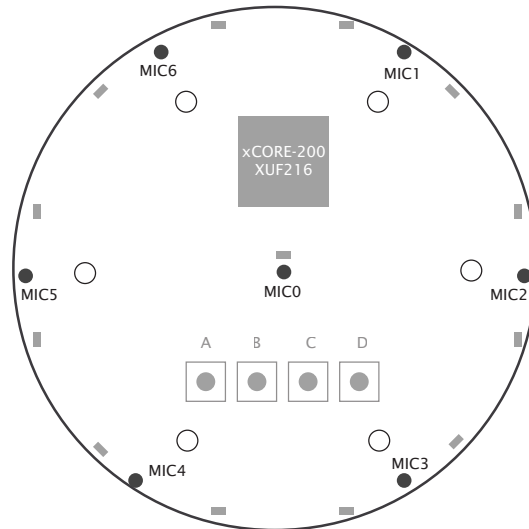


Figure 6:
MEMS
microphones

The microphone signals are mapped onto the xCORE-200 device as show in Figure 7:

Microphone	xCORE GPIO	Port
MIC_CLK	X0D12	P1E0
MIC_0	X0D14	P4C0
MIC_1	X0D15	P4C1
MIC_2	X0D16	P4D0
MIC_3	X0D17	P4D1
MIC_4	X0D18	P4D2
MIC_5	X0D19	P4D3
MIC_6	X0D20	P4C2

Figure 7:
MEMS
microphone
xCORE GPIO

6 Ethernet Connectivity

10/100 Mbps Ethernet connectivity consists of Microchip LAN8710A Ethernet PHY (U20) and an RJ45 connector (J3) with integrated magnetics. The PHY uses the 25MHz crystal as a reference clock.

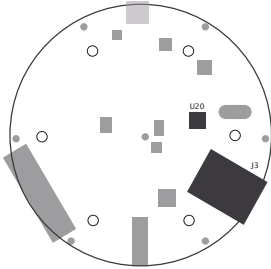


Figure 8:
Ethernet
components

The MII signals are mapped onto the xCORE-200 device as shown in Figure 9:

RGMI signal	xCORE GPIO	Port
RX_CLK	X1D00	P1A0
TX_CLK	X1D01	P1B0
RX0	X1D02	P4A0
RX1	X1D03	P4A1
TX0	X1D04	P4B0
TX1	X1D05	P4B1
TX2	X1D06	P4B2
TX3	X1D07	P4B3
RX2	X1D08	P4A2
RX3	X1D09	P4A3
RXDV	X1D10	P1C0
TXEN	X1D11	P1D0
MDC	X1D14	P4C0
MDIO	X1D15	P4C1
PLL_SYNC_OUT	X1D16	P4D0
ETH_RST_N	X1D29	P4F1
RXER	X1D35	P1L0

Figure 9:
Ethernet
xCORE GPIO

7 General purpose user interface

The board has 13 LEDs that are controlled by the xCORE-200 GPIO.

LED_0 - LED_11 (D2-D13) are positioned around the edge of the board, one each side of all every microphone.

The green LED (D14) in the middle of the board indicates a 3V3 power good signal.

Four general purpose push-button switches are provided. When pressed, the push-buttons create a connection from the I/O to GND. Care must be taken to ensure that this does not cause undesirable behavior on the xCORE-200 or other components connected through the GPIO headers.

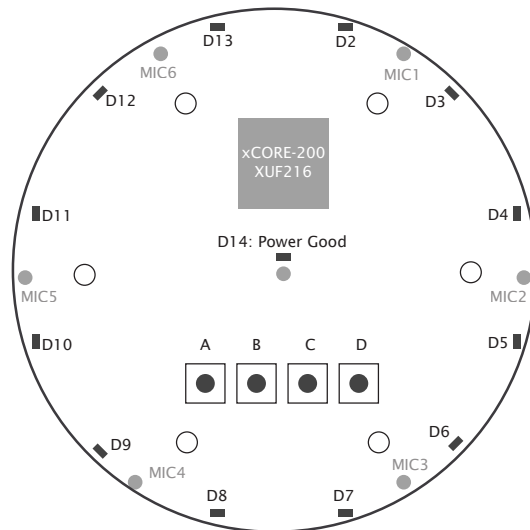


Figure 10:
General
purpose user
interface
components

The signal mapping of the user interface components is shown in Figure 11

UI signal	xCORE GPIO	Port
LED_0	X0D14	P4E0
LED_1	X0D15	P4E1
LED_2	X0D20	P4F0
LED_3	X0D21	P4F1
LED_4	X0D16	P4F2
LED_5	X0D17	P4F3
LED_6	X0D18	P4E2
LED_7	X0D19	P4E3
LED_8	X0D16	P1K0
LED_9	X0D17	P1L0
LED_10	X0D18	P1M0
LED_11	X0D19	P1N0
LED_12	X0D20	P1O0
LED_EON	X0D20	P1P0
BUTTON_A	X0D04	P4A0
BUTTON_B	X0D05	P4A1
BUTTON_C	X0D06	P4A2
BUTTON_D	X0D07	P4A3

Figure 11:
User interface
GPIO

8 USB Port

The micro-USB connector (J1) is connected to the USB PHY integrated in the XUF216 device, and provides power for the on-board circuits, and USB interface connectivity. Voltage tolerance should be as per USB VBUS specification values.

The power source is used to generate the following voltage rails:

- ▶ +1V0 (Core voltage to XMOS device)
- ▶ +2v5 (for headphone amplifier in DAC device)
- ▶ +3v3 for GPIOs and other accessory devices

Proper power-on sequence is indicated by power good LED (D1) in bottom side of the board.

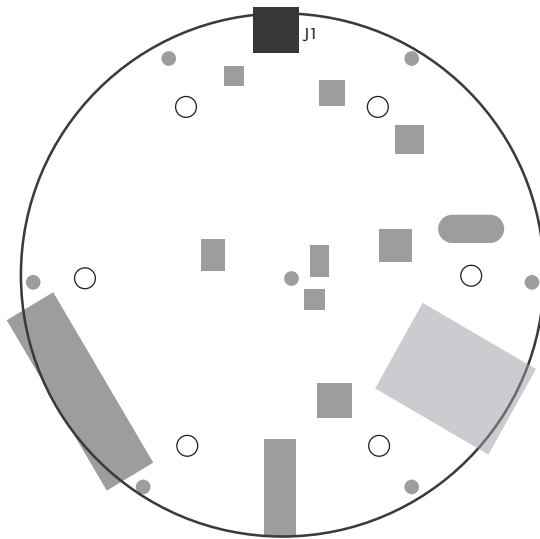


Figure 12:
USB
components

NOTE: J1 must be connected at all times to provide power to the xCORE-200 microphone array board.

9 Flash Memory

The XUF216-512-TQ128 device includes 2Mbytes of Quad Serial Peripheral Interface (QSPI) FLASH memory, which is interfaced by the GPIO connections shown in Figure 13:

QSPI connection	Pin	Port
QSPI_SS	X0D01	P1B
QSP_D0	X0D04	P4B0
QSP_D1	X0D05	P4B1
QSP_D2	X0D06	P4B2
QSP_D3	X0D07	P4B3
SPI_CLK	X0D10	P1C

Figure 13:
QSPI Flash

10 xSYS connector

A standard XMOS xSYS interface (J2) is provided to allow host debug of the board via JTAG.

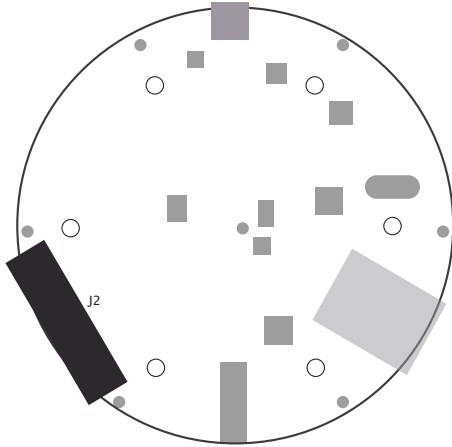


Figure 14:
xSYS
connector

XSYS signal	xCORE GPIO	Header pin	Description
TMS	See note	7	JTAG Test Mode Select.
TCK	See note	9	JTAG Test Clock.
TDI	See note	5	JTAG Test Data In. From debug adapter to XS1-U8.
TDO	See note	13	JTAG Test Data Out. From XS1-U8 to debug adapter.
RST_N	See note	15	System Reset. Active low, resets XS1-U8 device
GND		4, 8, 12, 16, 20	Ground.
XL_UP1	X0D43	6	XMOS link, uplink bit 1
XL_UP0	X0D42	10	XMOS link, uplink bit 0
XL_DN1	X0D40	14	XMOS link, downlink bit 1
XL_DN0	X0D41	18	XMOS link, downlink bit 0

Figure 15:
XSYS
Connector
Pinout

Notes:

- ▶ JTAG connections occupy dedicated connections

11 Power connector

xCORE-200 microphone array reference board requires a 5V power source input via the micro-USB cable - see USB Port above.

The voltage is converted by the on-board regulator to the 1V0, 2V5 and 3V3 supplies used by the components.

12 xCORE-200 Microphone Array Platform Portmap

The table below provides a full description of the port-pin mappings described throughout this document for the xCORE-200 Microphone Array Platform board.

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X0D00	1A ⁰					
X0D01	1B ⁰					QSPI_CS
X0D02		4A ⁰	8A ⁰	16A ⁰	32A ²⁰	BUTTON_A
X0D03		4A ¹	8A ¹	16A ¹	32A ²¹	BUTTON_B
X0D04		4B ⁰	8A ²	16A ²	32A ²²	QSPI_D0
X0D05		4B ¹	8A ³	16A ³	32A ²³	QSPI_D1
X0D06		4B ²	8A ⁴	16A ⁴	32A ²⁴	QSPI_D2
X0D07		4B ³	8A ⁵	16A ⁵	32A ²⁵	QSPI_D3
X0D08		4A ²	8A ⁶	16A ⁶	32A ²⁶	BUTTON_C
X0D09		4A ³	8A ⁷	16A ⁷	32A ²⁷	BUTTON_D
X0D10	1C ⁰					QSPI_CLK
X0D11	1D ⁰					
X0D12	1E ⁰					MIC_CLK
X0D13	1F ⁰					MCLK_XCORE
X0D14		4C ⁰	8B ⁰	16A ⁸	32A ²⁸	MIC_0_DATA
X0D15		4C ¹	8B ¹	16A ⁹	32A ²⁹	MIC_1_DATA
X0D16		4D ⁰	8B ²	16A ¹⁰		MIC_2_DATA
X0D17		4D ¹	8B ³	16A ¹¹		MIC_3_DATA
X0D18		4D ²	8B ⁴	16A ¹²		MIC_4_DATA
X0D19		4D ³	8B ⁵	16A ¹³		MIC_5_DATA
X0D20		4C ²	8B ⁶	16A ¹⁴	32A ³⁰	MIC_6_DATA
X0D21		4C ³	8B ⁷	16A ¹⁵	32A ³¹	
X0D22	1G ⁰					
X0D23	1H ⁰					
X0D24	1I ⁰					
X0D25	1J ⁰					
X0D26		4E ⁰	8C ⁰	16B ⁰		LED_0
X0D27		4E ¹	8C ¹	16B ¹		LED_1
X0D28		4F ⁰	8C ²	16B ²		LED_2
X0D29		4F ¹	8C ³	16B ³		LED_3
X0D30		4F ²	8C ⁴	16B ⁴		LED_4
X0D31		4F ³	8C ⁵	16B ⁵		LED_5
X0D32		4E ²	8C ⁶	16B ⁶		LED_6
X0D33		4E ³	8C ⁷	16B ⁷		LED_7
X0D34	1K ⁰					LED_8
X0D35	1L ⁰					LED_9
X0D36	1M ⁰		8D ⁰	16B ⁸		LED_10
X0D37	1N ⁰		8D ¹	16B ⁹		LED_11
X0D38	1O ⁰		8D ²	16B ¹⁰		LED_12
X0D39	1P ⁰		8D ³	16B ¹¹		LED_OEN
X0D40			8D ⁴	16B ¹²		XL_DN1
X0D41			8D ⁵	16B ¹³		XL_DN0
X0D42			8D ⁶	16B ¹⁴		XL_UP0
X0D43			8D ⁷	16B ¹⁵		XL_UP1

Figure 16:
xCORE-200
Microphone
Array
Platform
Portmap: Tile
0

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X1D00	1A ⁰					
X1D01	1B ⁰					
X1D02		4A ⁰	8A ⁰	16A ⁰	32A ²⁰	ETH_RXCLK
X1D03		4A ¹	8A ¹	16A ¹	32A ²¹	ETH_TXCLK
X1D04		4B ⁰	8A ²	16A ²	32A ²²	ETH_RXD_0
X1D05		4B ¹	8A ³	16A ³	32A ²³	ETH_RXD_1
X1D06		4B ²	8A ⁴	16A ⁴	32A ²⁴	ETH_TXD_0
X1D07		4B ³	8A ⁵	16A ⁵	32A ²⁵	ETH_TXD_1
X1D08		4A ²	8A ⁶	16A ⁶	32A ²⁶	ETH_TXD_2
X1D09		4A ³	8A ⁷	16A ⁷	32A ²⁷	ETH_TXD_3
X1D10	1C ⁰					ETH_RXD_2
X1D11	1D ⁰					ETH_RXD_3
X1D14		4C ⁰	8B ⁰	16A ⁸	32A ²⁸	ETH_RXDV
X1D15		4C ¹	8B ¹	16A ⁹	32A ²⁹	ETH_TXEN
X1D16		4D ⁰	8B ²	16A ¹⁰		
X1D17		4D ¹	8B ³	16A ¹¹		
X1D18		4D ²	8B ⁴	16A ¹²		SMI_MDC
X1D19		4D ³	8B ⁵	16A ¹³		SMI_MDIO
X1D20		4C ²	8B ⁶	16A ¹⁴	32A ³⁰	SYNC_OUT
X1D21		4C ³	8B ⁷	16A ¹⁵	32A ³¹	
X1D26		4E ⁰	8C ⁰	16B ⁰		I2C_SCLK
X1D27		4E ¹	8C ¹	16B ¹		I2C_SDA
X1D28		4F ⁰	8C ²	16B ²		DAC_RST_N
X1D29		4F ¹	8C ³	16B ³		ETH_RST_N
X1D30		4F ²	8C ⁴	16B ⁴		
X1D31		4F ³	8C ⁵	16B ⁵		
X1D32		4E ²	8C ⁶	16B ⁶		
X1D33		4E ³	8C ⁷	16B ⁷		
X1D35	1L ⁰					ETH_RX_ERR
X1D36	1M ⁰		8D ⁰	16B ⁸		I2S_BCLK
X1D37	1N ⁰		8D ¹	16B ⁹		I2S_LRCLK
X1D38	1O ⁰		8D ²	16B ¹⁰		MCLK
X1D39	1P ⁰		8D ³	16B ¹¹		I2S_DAC_DATA
X1D40			8D ⁴	16B ¹²		
X1D41			8D ⁵	16B ¹³		
X1D42			8D ⁶	16B ¹⁴		
X1D43			8D ⁷	16B ¹⁵		

Figure 17:
xCORE-200
Microphone
Array
Platform
Portmap: Tile
1

13 Operating requirements

A USB 2.0 high-speed compliant cable of less than 3m in length should be used when operating the xCORE-200 Microphone Array Reference Board. XMOS cannot guarantee correct operation of the xCORE-200 Microphone Array Reference Board should any other cable be used.

This product is, like most electronic equipment, sensitive to Electrostatic Discharge (ESD) events. Users should operate the xCORE-200 Microphone Array Reference Board with appropriate ESD precautions in place.

14 Dimensions

This microphone array reference board has diameter of 90 mm and board thickness of 1.6mm.

15 RoHS and REACH

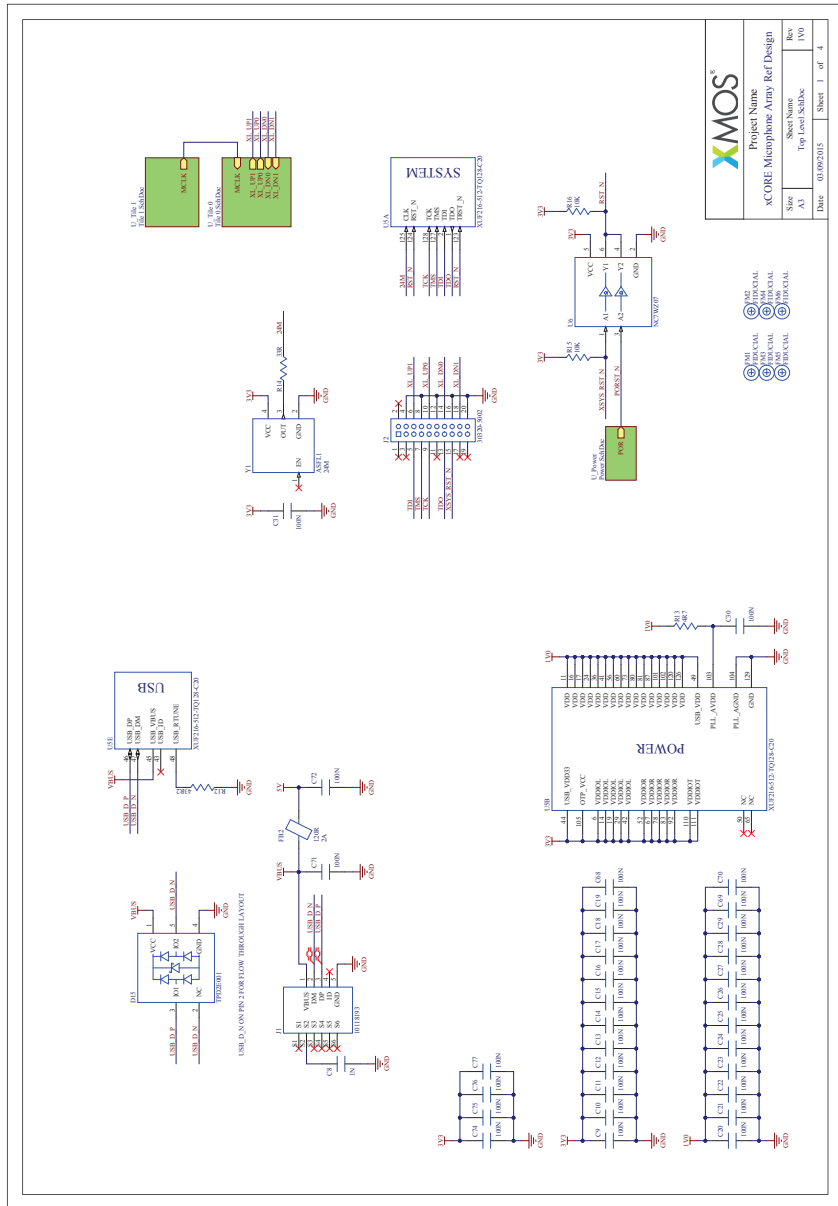
The xCORE-200 Microphone Array Reference Board complies with appropriate RoHS2 and REACH regulations and is a Pb-free product.

The xCORE-200 Microphone Array Reference Board is subject to the European Union WEEE directive and should not be disposed of in household waste. Alternative requirements may apply outside of the EU.



16 Schematics

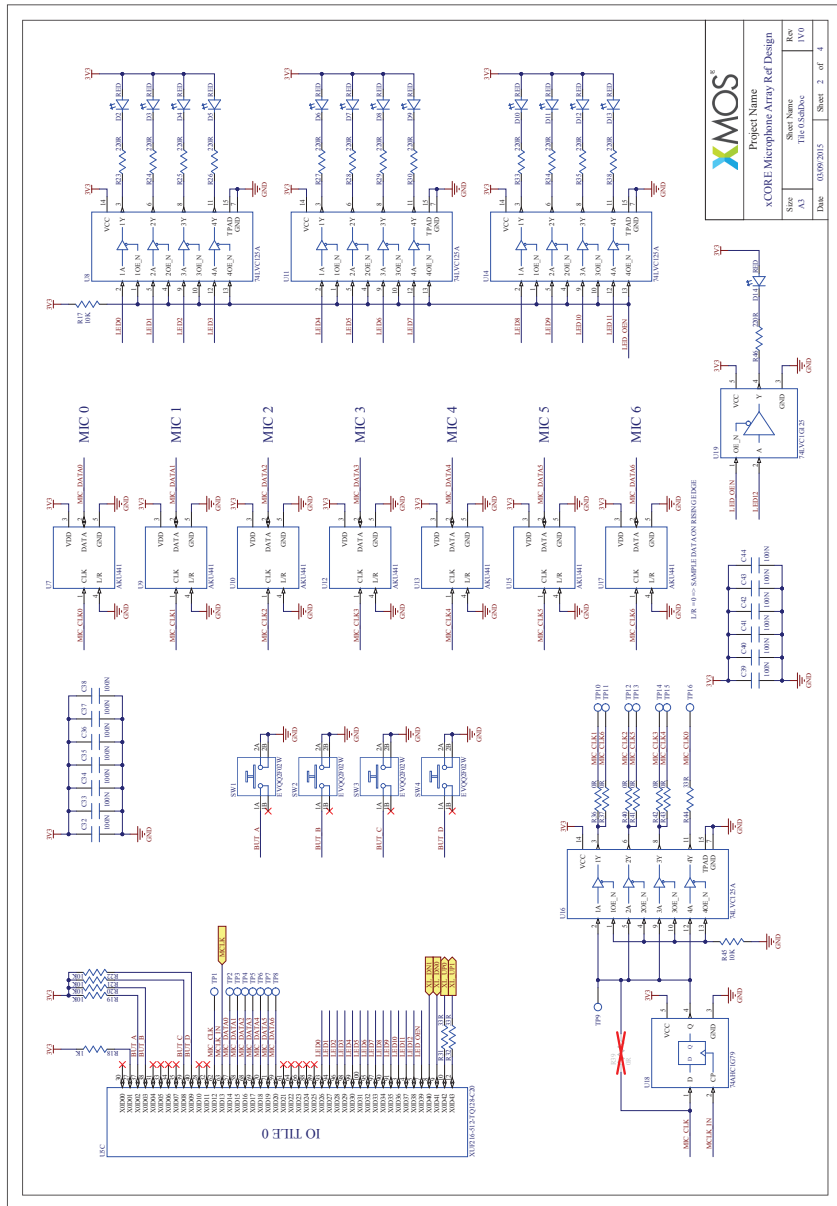
Figure 18:
Microphone
Array
Reference
Board - Power
entry and
xCORE-200
Configura-
tion



XMOS
Project Name
xCORE Microphone Array Ref Design

Sheet Name	Rev
01	1.0
Top Level Schematic	
Date	06/09/2015
Sheet	1 of 4

Figure 19:
Microphone
Array
Reference
Board -
Microphone



		Project Name	
		xCORE Microphone Array Ref Design	
Sheet Name	Sheet No.	Row	Col
17	14	1	1
Date	06/05/2015	Sheet 2 of 4	

Figure 20:
Microphone
Array
Reference
Board -
Ethernet and
Stereo DAC
with
Headphone
Jack circuitry

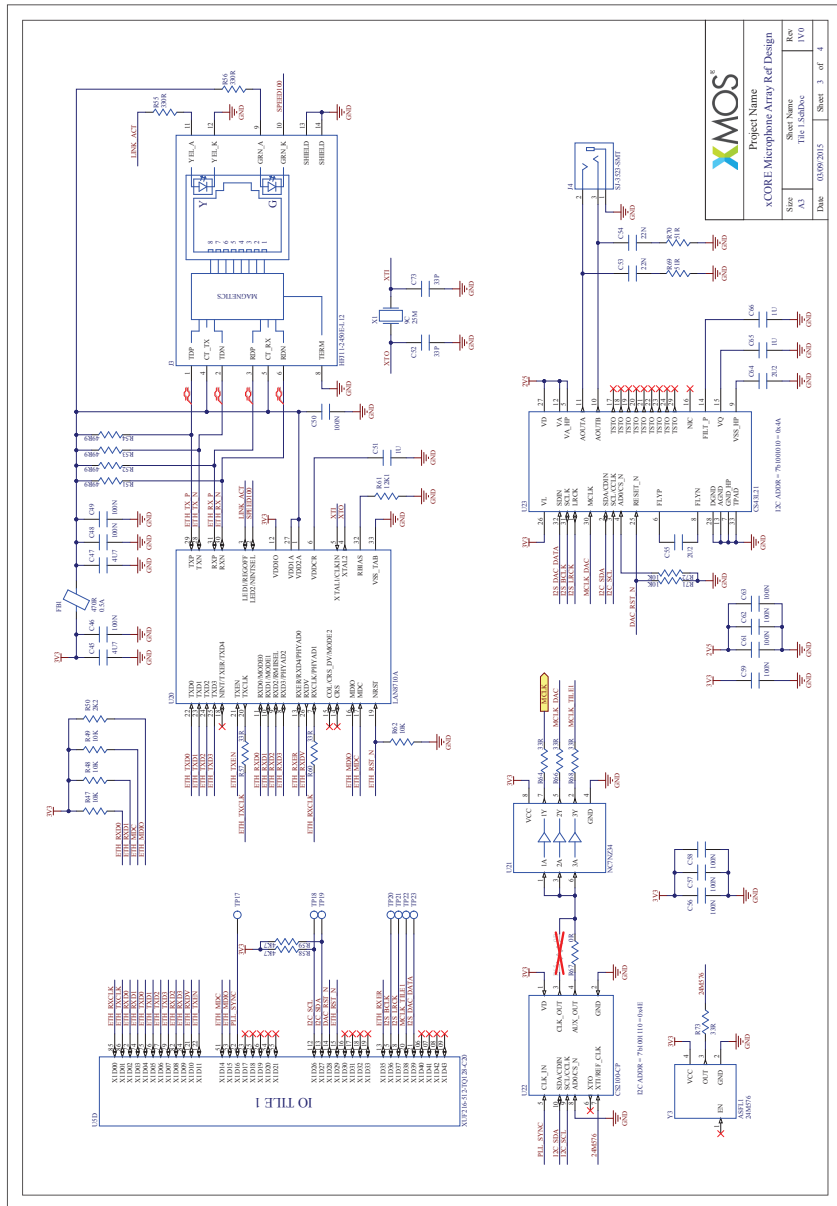
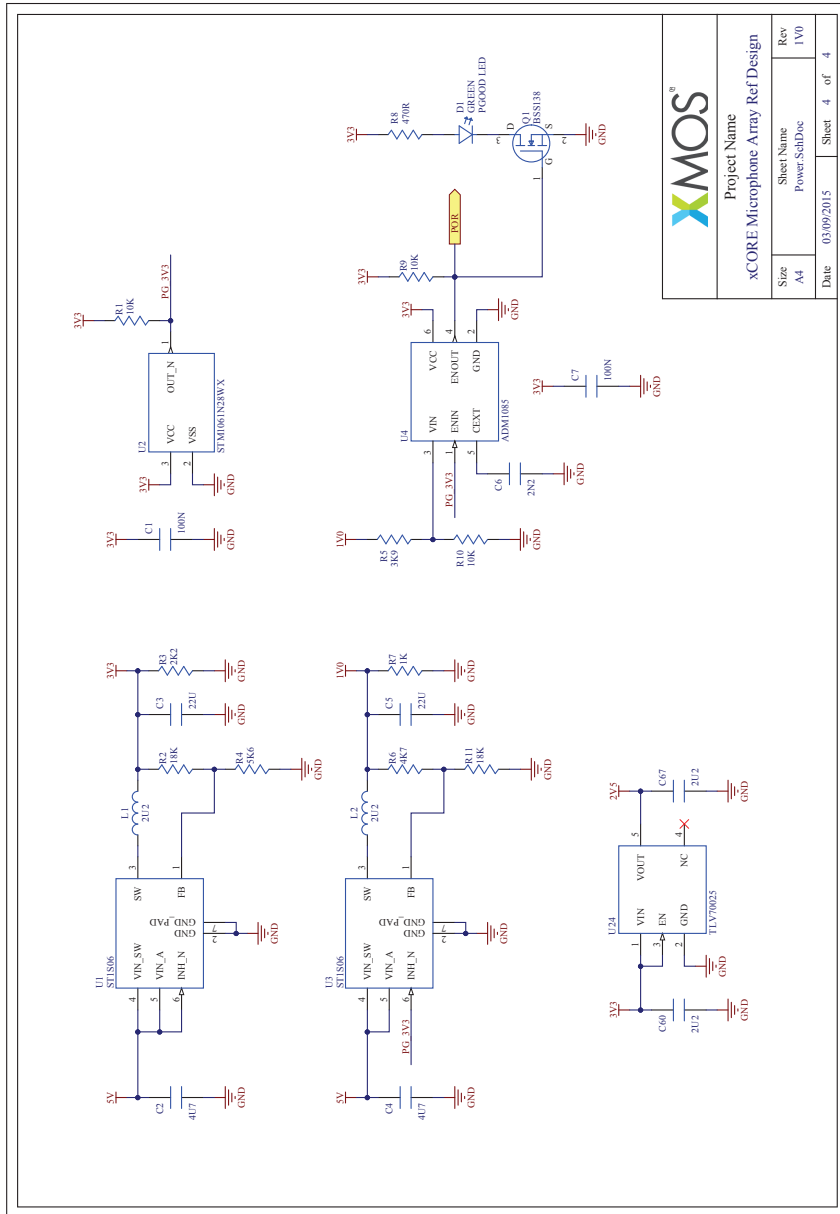


Figure 21:
Microphone
Array
Reference
Board -
Voltage rail
LDOs and
reset circuit



XMOS	
Project Name xCORE Microphone Array Ref Design	
Size A4	Sheet Name Power:SubDoe
Rev 1V0	Date 03/09/2015
Sheet 4 of 4	



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