version1.1.1scopeExample. This code is provided as example code for a user to base
their code on.descriptionHow to input data accompanied by a data valid signalboardsUnless otherwise specified, this example runs on the SliceKIT Core
Board, but can easily be run on any XMOS device by using a different
XN file.

A clocked port can interpret a readyln strobe signal that determines the validity of the accompanying data. The example below inputs data from a clocked port only when a readyln signal is high.

The following statement configures the input port inP to be sampled only when the value sampled on the port inReady equals 1. The readyIn port must be 1-bit wide.

configure_in_port_strobed_slave(inP, inReady, clk);

Data is sampled on the rising edge of the clock whenever the ready-in signal is high. The port samples two 4-bit values and combines them to produce a single 8-bit value for input by the processor.

inP :> void;

Publication Date: 2013/11/15

XMOS © 2013, All Rights Reserved

Xmos Ltd. is the owner or licensee of the information in this document and is providing it to you "AS IS" with no warranty of any kind, express or implied and shall have no liability in relation to its use. Xmos Ltd. makes no representation that the information, or any particular implementation thereof, is or will be free from any claims of infringement and again, shall have no liability in relation to any such claims.



REV A