XVF3615 Voice Processor - Datasheet

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The VocalFusion® XVF3615 is a high-performance voice processor, derived from XMOS xcore.ai, that is optimised for integrated and accessory voice interface applications.

Important:

The information in this datasheet should be read in conjunction with the **XU316-1024-QF60(A/B)** datasheets which contains electrical, design and integration data for the base processor.

xcore.ai base datasheet links:

XU316-1024-QF60A

XU316-1024-QF60B

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1 Key features

The VocalFusion® XVF3615 is a high-performance voice processor that is optimised for integrated applications.

The XVF3615 has the following key features:

1.1 Voice Processing

- Two PDM microphone interfaces
- Digital signal processing pipeline
- Full duplex, stereo, Acoustic Echo Cancellation (AEC)
- Reference audio via I^2S with automatic bulk delay insertion
- Point noise suppression via interference canceller
- Switchable stationary noise suppressor
- Programmable Automatic Gain Control (AGC)
- Flexible audio output routing and filtering
- Independent audio paths for communications and Automatic Speech Recognition (ASR), and embedded Amazon Wake Word feature.

1.2 Device Interfaces

- Full speed USB2.0 compliant device supporting USB Audio Class (UAC) 1.0
- USB HID and Endpoint 0 control interfaces
- Flexible Peripheral Interfaces
- Programmable digital general-purpose inputs and outputs
- I^2C interface for system control and local peripheral control
- I^2S Slave interface input & output of audio data
- SPI Master interface for control and interrogation of local SPI slave devices

1.3 Firmware Management

- Boot from QSPI Flash
- Default firmware image for power-on operation
- Persistent user data maintained across firmware upgrade cycles
- User-programmable setup for SPI peripherals
- Option to boot from a local host processor via SPI
- Device Firmware Update (DFU) via I^2C or USB

1.4 Package

- 7mm x 7mm 60pin QFN package

1.5 Power Consumption

- Typical power consumption 300-350mW

2 Product overview

2.1 Scope

The XMOS VocalFusion® XVF3615 voice processor uses microphone array processing to capture clear, high-quality audio from anywhere in the room. XVF3615 processors use highly optimised digital signal processing algorithms to implement 'barge-in', suppress point noise sources and reduce ambient noise levels increasing the effective Signal to Noise Ratio (SNR) to achieve a reliable voice interface whatever the environment.

The processor is designed for seamless integration into consumer electronic products requiring voice interfaces for Automatic Speech Recognition (ASR), or communication and conferencing. In addition to the class-leading voice processing, XVF3615 processor implements specific features and interfaces required for use in closely integrated applications such as those incorporated into a TV or set-top box.

Three modes of operation are supported by the XVF3615:

- XVF3615-UA (**U**-SB **A**-ccessory) - Audio and control via a USB2.0 interface
- XVF3615-UA-HYBRID (**U**-SB **A**-ccessory **HYBRID**) - Audio to the host and control via a USB2.0 interface, audio from the host via I^2S master interface
- XVF3615-INT (**INT**-egrated) – Audio via I^2S and control over I^2C interfaces

The functional block diagram of the XVF3615 is shown in the figures below:

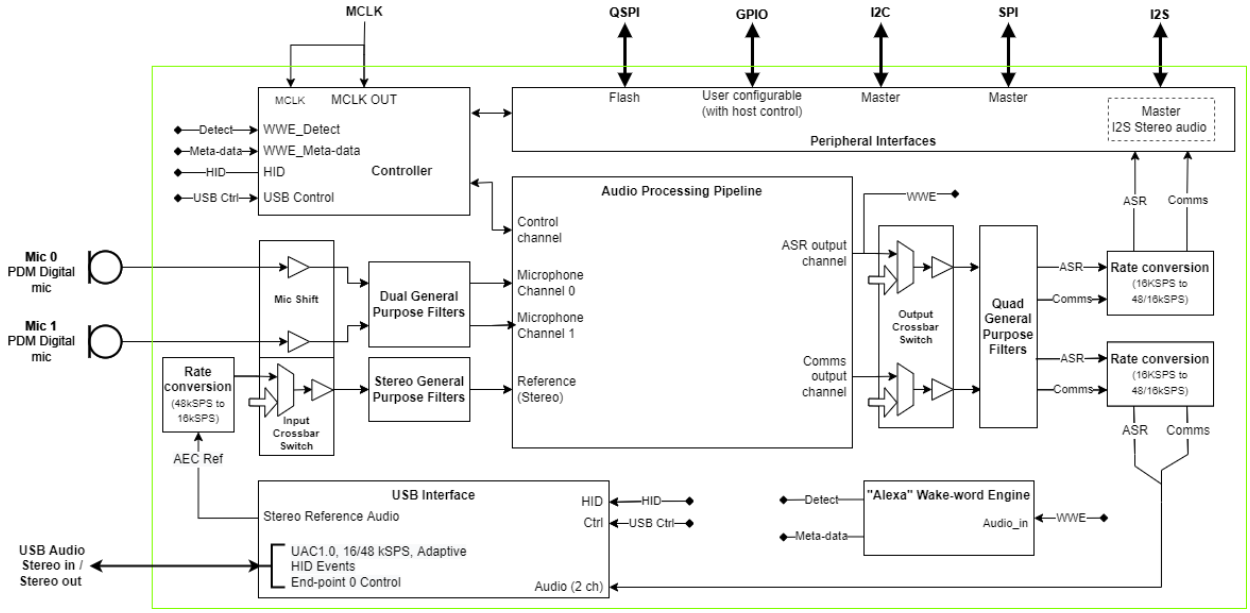

Fig. 2.1: Functional block diagram of XVF3615 in UA configuration

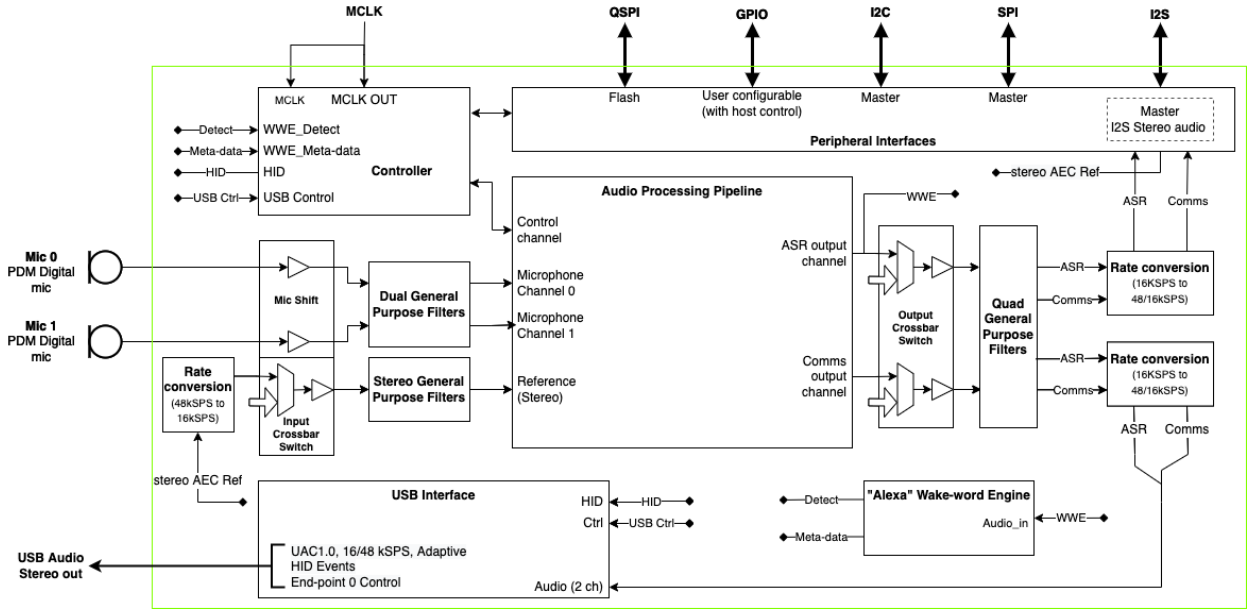

Fig. 2.2: Functional block diagram of XVF3615 in UA-HYBRID configuration

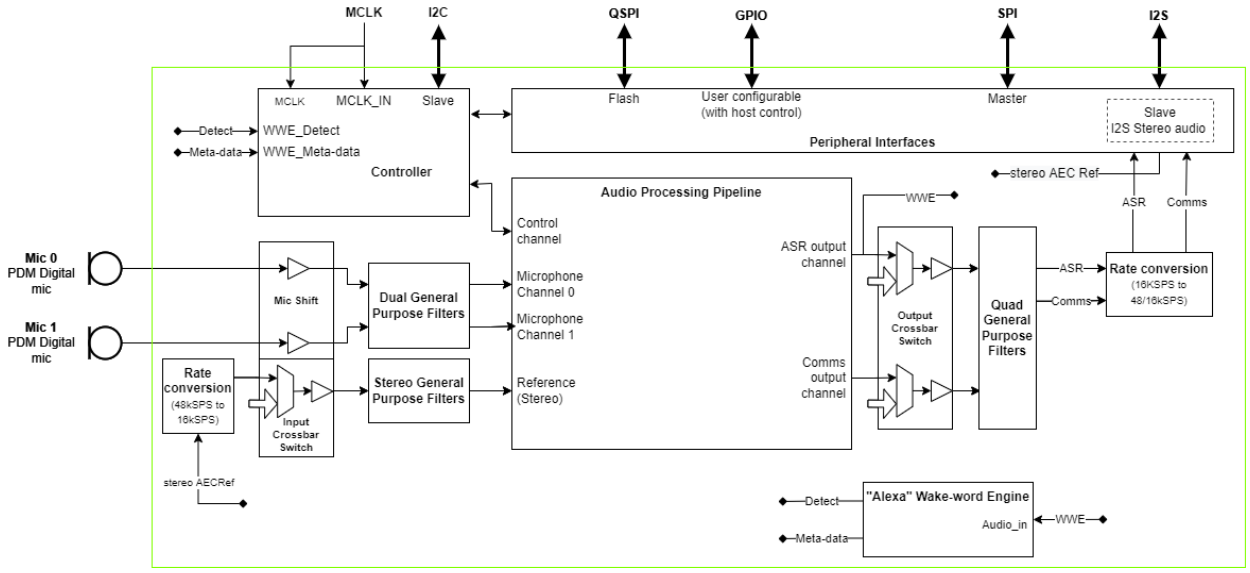

Fig. 2.3: Functional block diagram of XVF3615 in INT configuration

2.2 Audio Processing

The VocalFusion® XVF3615 voice processor converts and enhances audio captured using a pair of low-cost digital microphones. Processed audio streams are suitable for use in Automatic Speech Recognition or voice communications applications and benefit from a range of configurable audio processing techniques to allow customisation to the use case. The embedded audio processing provides the following features:

- 2 microphone far-field operation.
- Full 360-degree operation in “coffee table” applications or 180 degree for operation in edge-of-room products such as smart TVs.
- 16kHz voice processing, with optional 16kHz and 48kHz interface sample rates.
- Full duplex, Stereo, Acoustic Echo cancellation with a maximum tail length of 225ms accommodating highly reverberant environments. The reference audio for cancellation can be provided via an I^2S Slave interface (INT variant), I^2S Master interface (UA-HYBRID variant) or via USB (UA variant).
- Automatic bulk delay insertion, of up to 150ms, to account for positive or negative reference audio delays ensuring optimal echo cancellation with all audio output paths.
- Cancellation of point noise sources via a 256-frequency band Interference Canceller.
- Switchable stationary noise suppressor.
- Adjustable gain over a 60dB range with automatic gain control.
- Audio output filtering and range limiter.
- Independent audio paths for communications and Automatic Speech Recognition (ASR), and embedded Amazon Wake Word feature.

2.3 Peripheral interfaces

The VocalFusion® XVF3615 voice processor provides the following additional interfaces to increase usability and reduce total system cost:

- 4 General Purpose Output pins. These can be configured as simple digital I/O pins, Pulse Width Modulated (PWM) outputs and rate adjustable LED flashers.
- 4 General Purpose Input pins. These can be used as simple logic inputs or event capture (edge detection).
- SPI Master interface to control and interrogate an SPI Slave device, such as ADCs, DACs or external keyword detection devices.

2.4 System firmware

Note: The three XVF3615 configurations; one providing I^2S/I^2C interface (XVF3615-INT) and two providing a USB interface (XVF3615-UA and XVF3615-UA-HYBRID) are delivered as separate sets of firmware.

The VocalFusion® XVF3615 voice processor can be booted over SPI by a local host processor or from a separate, user-supplied, QSPI Flash memory. When operating with flash, the memory can be used for the following functions:

- A default firmware image for power-on operation.
- An upgrade image. Upgrades are provided via I^2C or USB providing a host-controlled upgrade process for over-the-air device management.
- A persistent user information space to allow user-configured data such as board identifiers and serial numbers to be maintained across multiple firmware upgrade cycles.
- An upgradable user command space. Commands stored in this space are executed at boot time allowing the definition of start-up behaviour, VocalFusion® XVF3615 configuration and setup of SPI peripheral devices connected to it.

With the exception of the persistent user information, the contents of the flash, and therefore the configuration of the system, can be upgraded and configured using the Device Firmware Upgrade (DFU) mechanism from the host processor.

3 Audio Processing

3.1 Signal processing pipeline

The XVF3615 audio processing pipeline takes inputs from a pair of MEMS Pulse Density Modulation (PDM) microphones and uses advanced signal processing to create audio streams suitable for use in Automatic Speech Recognition (ASR) and voice communication applications. The block diagram of this audio processing pipeline is shown in the figure below.

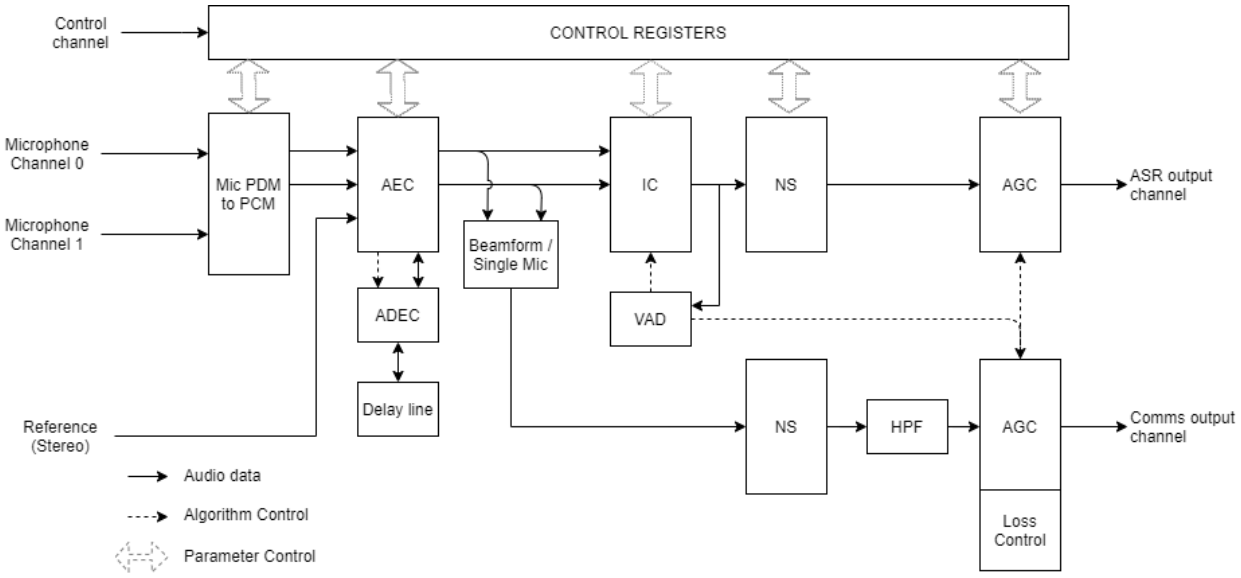

Fig. 3.1: The XVF3615 audio processing pipeline

The pipeline enhances the captured audio stream using a set of complementary signal enhancement and noise reduction processes:

- **Microphone PDM to Pulse Code Modulation (PCM) conversion:** converts the PDM audio input from the microphones into PCM format allowing further processing.
- **Acoustic Echo Cancellation (AEC):** enables the XVF3615 to detect voice signals in the presence of high volume, stereo audio from the product into which it is integrated. This process takes the stereo audio from the product as a reference signal and models the echo characteristics between each speaker and microphone caused by the acoustic environment of the device and room. The models are used to remove the echos present in the microphone audio inputs. The models are continuously adapted to the acoustic environment to accommodate changes in the room created by events such as doors opening or closing and people moving in the room.
- **The Automatic Delay Estimation Control (ADEC):** automatically monitors and manages the delay between the reference audio and the echo received by the microphone to ensure optimal AEC cancellation when the audio output latency is variable or non-zero.
- **Interference Cancellation (IC):** suppresses static noise from point sources such as cooker hoods, washing machines, or radios for which there is no reference audio signal available. When an internal Voice Activity Detector (VAD) indicates the absence of voice, the IC adapts to suppress point noise sources in the environment. When voice is detected adaption is suspended maintaining suppression of the interfering noise source.
- **Noise Suppression (NS):** suppresses diffuse noise from sources whose frequency characteristics do not change rapidly over time such as air conditioning or city background noise.

- **Automatic Gain Control (AGC):** tunes separate AGC channels for Automatic Speech Recognition and communications output. The internal VAD is used to prevent gain changes in the ASR output channel during speech to improve speech recognition performance.

3.2 Reference signal delay

As shown above, the XVF3615 includes an Automatic Delay Estimator Control(ADEC) which is used to time-align the reference and microphone signals, allowing the Acoustic Echo Canceller (AEC) to work effectively. This is an essential aspect of device operation for situations where the audio output path is unknown, such as in TVs and set-top box architectures.

The ADEC applies a time shift to one of the signals based on an automatic estimate between them, or a user-defined delay, to deliver a synchronised input to the AEC.

A delay of between 0-150ms can be applied to either the reference signal or microphone input, equivalent to 0-2400 samples at 16kHz sample frequency.

The ADEC runs in one of three modes:

1. **Automatic** - the ADEC runs immediately after the device starts. It constantly monitors the reference signal and microphone input for changes of time alignment and automatically adjusts its delay as necessary.
2. **Manual** – in this mode, the ADEC waits in a disabled state until the device is manually triggered by the host. The delay is estimated at the trigger point, or a selected fixed delay applied. The delay set will be used until it is changed by:
    - manually applying a different fixed delay.
    - manually triggering a new delay estimate.
    - switching to automatic mode.
3. **Estimate on Start-up** (default) - The ADEC runs immediately after the device starts, calculates the delay between the two signals and applies that delay to all subsequent signals. After making the initial delay estimate and delay setting, no further changes will be made unless manually triggered or automatic mode is selected.

For further information on the usage of ADEC please refer to the XVF3615 user guide.

3.3 Example applications

The essential components and signals for a XVF3615-INT application using QSPI flash memory with 1V8 I/0 is shown in the figure below.

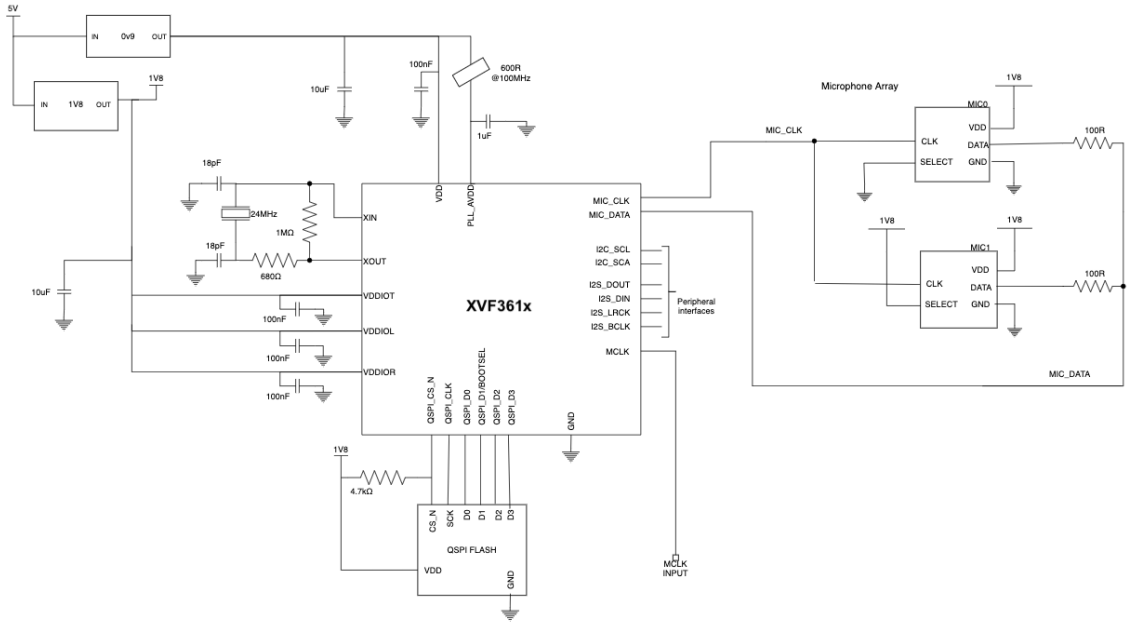

Fig. 3.2: Essential components of an XVF3615-INT application with VDDIO = 1V8

The essential components and signals for a XVF3615-UA application with 3V3 I/0 is shown in the figure below.

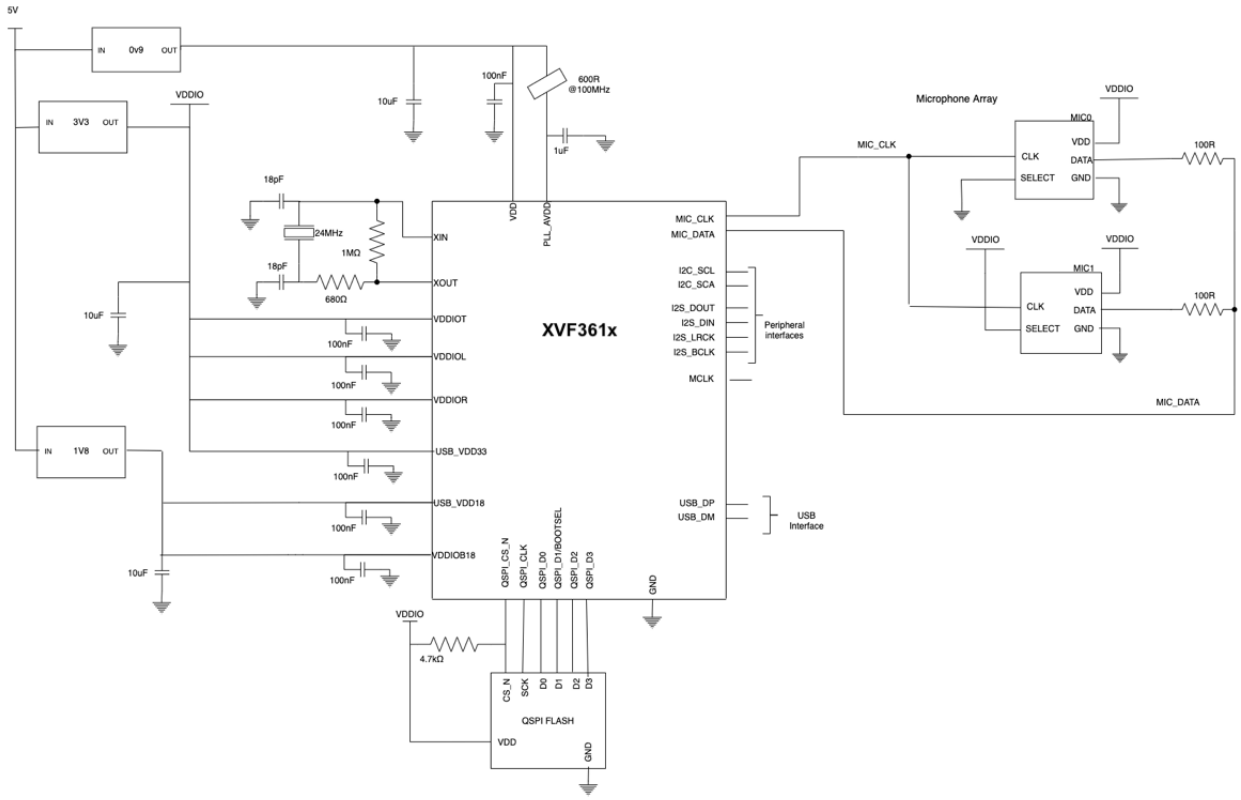

Fig. 3.3: Essential components of an XVF3615-UA application with 3V3 IO

4 Pin diagram

4.1 Pin configuration

The pinout of the XVF3615, including all optional interfaces, is shown in the figure below.

Pins marked *RESERVED* are internally connected and should remain unconnected.

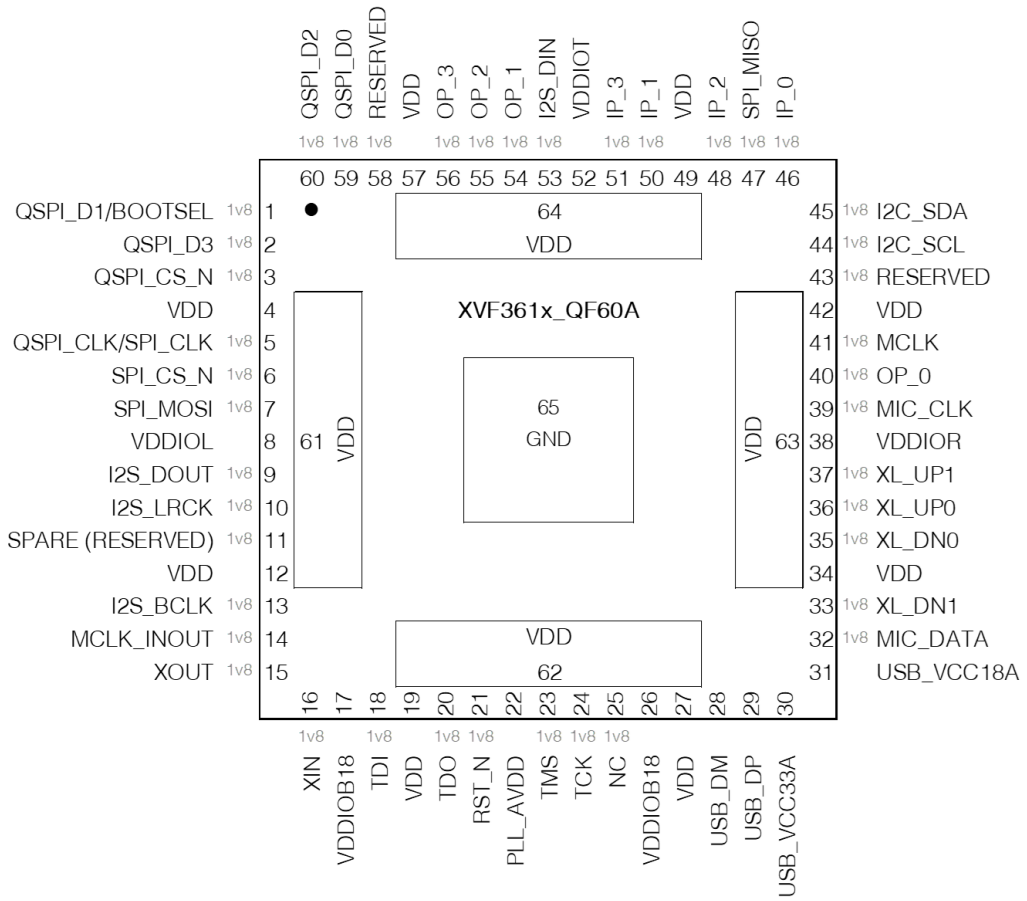

Fig. 4.1: XVF3615-QF60A pin configuration

Note:

Two package variants are available:

XVF3615-QF60A – (1V8 I/0) – VDDIOT, VDDIOL and VDDIOR should be connected a 1V8 supply
XVF3615-QF60B – (3V3 I/0) – VDDIOT, VDDIOL and VDDIOR should be connected a 3V3 supply

In both variants, VDDIO18 must be connected to a 1V8 supply and all VDD pins must be connected to a 0V9 supply. All package paddles (pins 61 to 65) must be connected. It is advised that vias be placed under paddles to connect directly to PCB supply planes

4.2 Signal description

The table below lists the functions of all the pins shown in Fig. 4.1 above in the order they appear around the package.

Note:

The function of some pins changes depending on the firmware configuration loaded during boot (INT/UA).

Table 4.1: XVF3615-QF60A pin table

Pin	Port	Name	Description	Comments	Direction	Power rail
1	X0D05	QSPI_D1 / BOOTSEL	QSPI Data Line 1 and boot selection.	If pin is tied high via a 4.7k ohm resistor on startup the device will start in SPI slave boot mode. If the pin is left floating or connected to a quad SPI D1 pin on a memory device, the device will start in QSPI Master mode and attempt to boot from the QSPI flash memory.	I / O	IOL
2	X0D07	QSPI_D3	QSPI Data Line 3		I / O	IOL
3	X0D01	QSPI_CS_N	QSPI Boot Flash - Chip Select	Pull high externally to the device using a 4.7k ohm resistor	O	IOL
5	X0D10	QSPI_CLK / SPI_CLK	QSPI Clock		O	IOL
6	X0D00	SPI_CS_N	Slave SPI boot / Peripheral SPI Master Chip Select	Pull high externally to the device using a 4.7k ohm resistor	I	IOL
7	X0D11	SPI_MOSI	SPI Master Out Slave In		I	IOL
8	VDDIOL	VDDIOL	I/O Power Supply (1v8)	All VDD pins must be connected.	PWR	NA
9	X1D00	I2S_DOUT	I2S Data Out	Audio data out	O	IOL
10	X1D01	I2S_LRCK	I2S Left/Right clock	48kHz or 16kHz clock derived as I2S_BLCK/64.	O (master), I (slave)	IOL
11	X1D09	SPARE (RESERVED)				IOL

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Table 4.1 – continued from previous page

Pin	Port	Name	Description	Comments	Direction	Power rail
13	X1D10	I2S_BCLK	I2S bit synchronisation clock	Configurable for 16kHz (1.024MHz) and 48kHz (3.072MHz) sample rates	O (master), I (slave)	IOL
14	X1D11	MCLK_INOUT	Master audio clock	Input in INT config; output in USB configs. Should be connected to Pin 41	I / O	IOL
15	XOUT	XOUT	Crystal oscillator output	Note that this pin should be left floating when using the CMOS clock input	O	IOB
16	XIN	XIN	Crystal oscillator input or CMOS clock input	alternatively this can be used as a clock input	I	IOB
17	VDDIOB18	VDDIOB18	I/O Power Supply (1v8)	All VDD pins must be connected.	PWR	NA
18	TDI	TDI	JTAG test data input	This pin has a weak internal pull-up. See note on debug headers.	I	IOB
20	TDO	TDO	JTAG test data output	See note on debug headers.	O	IOB
21	RST_N	RST_N	Device reset	Active low. This pin has a Schmitt trigger input and an internal weak pull up	I	IOB
22	PLL_AVDD	PLL_AVDD	Analogue power supply for core and application PLL.	Use a filtered version of the core supply, as per the XU316-1024-QF60A datasheet.	PWR	
23	TMS	TMS	JTAG test mode select	This pin has a weak internal pull-up. See note on debug headers..	I	IOB
24	TCK	TCK	JTAG test clock input	This pin has a Schmitt trigger input and an internal weak pull-down. See note on debug headers.	I	IOB
25	NC	NC		Not connected. This pin should NOT be connected to any net		IOB
26	VDDIOB18	VDDIOB18	I/O Power Supply (1v8)	All VDD pins must be connected.	PWR	NA
28	USB_DM	USB_DM		USB D- line. May be left floating if USB is not required		
29	USB_DP	USB_DP		USB D+ line. May be left floating if USB is not required		
30	USB_VDD33A	USB_VCC33A		USB 3.3V power for the USB transceiver. May be left floating if USB is not required	PWR	
31	USB_VDD18A	USB_VCC18A		USB 1.8V power for the USB transceiver. May be left floating if USB is not required	PWR	

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Table 4.1 – continued from previous page

Pin	Port	Name	Description	Comments	Direction	Power rail
32	X1D13	MIC_DATA	PDM microphone input	Note that this is a DDR input permitting a pair of digital DDR microphones to share this input	I	IOR
33	X1D16	XL_DN1	XLINK	These 4 signals form a single 2-wire xlink connection for advanced debug only. Do not connect in production desings.	I	IOR
35	X1D17	XL_DN0	XLINK		I	IOR
36	X1D18	XL_UP0	XLINK		O	IOR
37	X1D19	XL_UP1	XLINK		O	IOR
38	VDDIOR	VDDIOR	I/O Power Supply (1v8)	All VDD pins must be connected.	PWR	NA
39	X1D22	MIC_CLK	Microphone clock output.	3.072MHz	O	IOR
40	X0D29	OP_0	General purpose output	Eval kit - Used as interupt to the RaPi, via an I2C expander.	O	IOR
41	X0D35	MCLK	Master audio clock		I	IOR
43	X0D36	RESERVED		Leave this pin unconnected	I	IOR
44	X0D37	I2C_SCL	I2C serial clock line for receiving control command from I2C host		I / O	IOR
45	X0D38	I2C_SDA	I2C serial data line for receiving control command from I2C host		I / O	IOR
46	X0D40	IP_0		Eval kit Mute	I	IOT
47	X0D39	SPI_MISO	SPI Master In Slave Out	May be left floating if not required	O	IOT
48	X0D42	IP_2		General purpose input	I	IOT
50	X0D41	IP_1		Eval kit BUTTON	I	IOT
51	X0D43	IP_3		General purpose input	I	IOT
52	VDDIOT	VDDIOT	I/O Power Supply (1v8)	All VDD pins must be connected.	PWR	NA
53	X1D34	I2S_DIN	Peripheral I2S interface - I2S data input		I	IOT
54	X0D30	OP_1	General purpose output	Eval kit - LED_R	O	IOT
55	X0D31	OP_2	General purpose output	Eval kit - LED_G	O	IOT
56	X0D32	OP_3	General purpose output	Eval kit - Test point (and DAC reset if no-fit resistor fitted)	O	IOT
58	X0D33	RESERVED		Leave this pin unconnected		IOT
59	X0D04	QSPI_D0	QSPI Boot Flash / QSPI Data Line 0		I / O	IOL
60	X0D06	QSPI_D2	QSPI Data Line 2		I / O	IOL

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Table 4.1 – continued from previous page

Pin	Port	Name	Description	Comments	Direction	Power rail
65	GND	GND	Ground	All package paddles must be connected. It is advised that vias be placed under paddles to connect directly to PCB supply planes	GND	NA
61, 62, 63, 64	VDD	VDD	Core power supply (0v9)	All package paddles must be connected. It is advised that vias be placed under paddles to connect directly to PCB supply planes	PWR	NA
4, 12, 19, 27, 34, 42, 49, 57	VDD	VDD	Core power supply (0v9)	All VDD pins must be connected.	PWR	NA

A. All VDD pins must be connected, excluding the USB_VDD supplies which can be left floating if USB is not required.

B. Two package variants are available:
QF60A – (1V8 I/0) – VDDIOT, VDDIOL and VDDIOR must be connected a 1V8 supply
QF60B – (3V3 I/0) – VDDIOT, VDDIOL and VDDIOR must be connected a 3V3 supply

C. In both variants, VDDIO18 must be connected to a 1V8 supply.

D. All package paddles must be connected. It is advised that vias be placed under paddles to connect directly to PCB supply planes

5 Device interfaces

5.1 PDM microphone inputs

Two standard PDM MEMS microphones should be connected to the MIC_DATA pin. The data input makes use of the left and right channel output capability of standard MEMS microphones and the microphone data is read on alternative edges of the MIC_CLK signal. The XVF3615 reads one microphone on the positive edge of the microphone clock and the other microphone on the negative edge of the clock.

The XVF3615 outputs a microphone clock at 3.072MHz on the MIC_CLK output, which must be fed directly to both microphones. This signal must be used to clock the microphone PDM output to avoid undefined artefacts in the processed audio stream. One microphone should be set to be left (output on rising edge of clock) and the other right (output on the falling edge of clock).

An example microphone circuit is shown in the figure below:

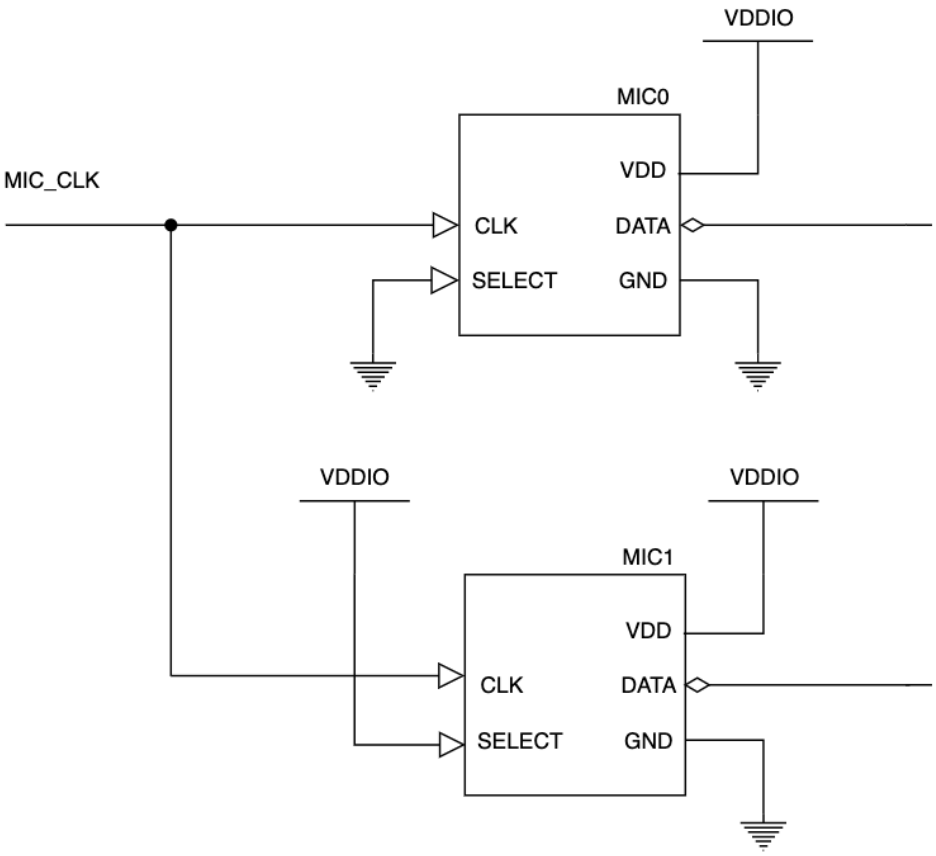


Fig. 5.1: PDM microphone schematic

The voice processor has been tested and characterised with microphones placed with a 71mm separation and connected to the product enclosure in such a way that the acoustic path to each microphone from outside the product is independent. The XVF3615 algorithms automatically adapt to alternative spacing, but differences in audio performance may occur and should be thoroughly characterised.

5.2 QSPI Boot mode

When QSPI boot mode is enabled (default), the XVF3615 enables the six QSPI pins, see table below, and drives the QSPI clock as a QSPI Master. A READ command is issued with a 24-bit address 0x000000.

Table 5.1: QSPI signals

Signal	Description	Comment	Pin	I/O
QSPI_CS_N	QSPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	3	O
QSPI_CLK / SPI_CLK	QSPI Clock		5	O
QSPI_D0	QSPI Data Line 0		59	I/O
QSPI_D1 / BOOT-SEL	QSPI Data Line 1	If pin is tied high via a 4.7k ohm resistor on startup and boot selection - the device will start in SPI Slave boot mode. If the pin is left floating pulled low or connected to a quad SPI D1 pin on a memory device - the device will start in QSPI Master mode and attempt to boot from a local QSPI flash memory	1	I/O
QSPI_D2	QSPI Data Line 2		60	I/O
QSPI_D3	QSPI Data Line 3		2	I/O

The XVF3615 expects each byte to be transferred with the least-significant nibble first. Programmers that write bytes into a QSPI interface using the most significant nibble first may have to reverse the nibbles in each byte of the image stored in the QSPI device. When bulk programming flash devices the Quad Enable bit in the flash setting register should be set.

For further information about the boot sequence refer to the XU316-1024-QF60(A/B) datasheet.

5.3 SPI Interface

The SPI interface can be utilised in both Master and Slave configurations for peripheral control of components like DACs and ADCs (Master), and SPI boot from host a host processor (Slave).

5.3.1 Peripheral component control

Once the XVF3615 has successfully booted, the SPI interface can be used to configure peripheral components such as DACs, ADCs and keyword detection devices. In this mode the SPI interface operates as a master, and transfers data held in flash, or received from the host over the control interface. The interface operates with the following specifications:

- 1MHz SPI clock
- Up to 128 bytes SPI write
- Up to 56 bytes SPI read

For further information on this configuration consult the XVF3615 user guide.

5.3.2 SPI Slave boot

To enable the SPI boot from an external host processor, the QSPI_D1/BOOTSEL should be pulled to VDDIO on power-up. This activates the SPI interface, which operates as a slave to the host processor for the transfer of the boot image, which is clocked in with the least significant bit first in each transferred byte.

This is an alternative to using an attached QSPI flash to automatically transfer boot data on start-up.

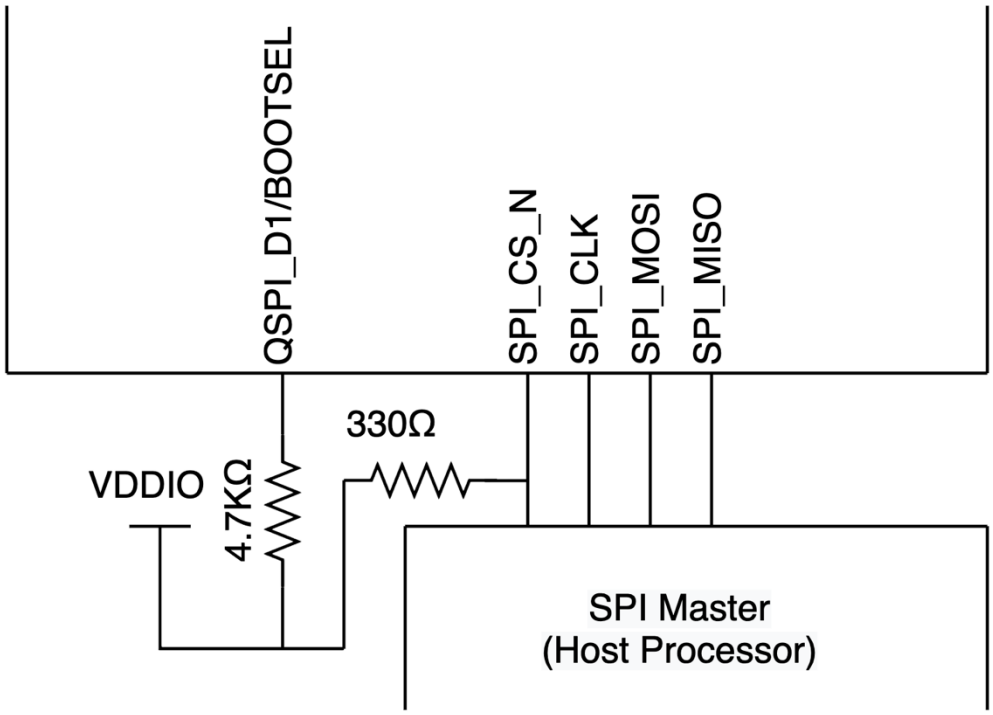


Fig. 5.2: XVF3615 SPI Slave boot configuration

The SPI pins are shown below in the table below.

Table 5.2: SPI signals

Signal	Description	Comment	Pin	I/O
SPI_CLK	SPI Clock		5	I
SPI_CS_N	SPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	6	I
SPI_MOSI	SPI Master Out Slave In		7	I
SPI_MISO	SPI Master In Slave Out	May be left floating if not required	47	O

5.4 Integrated USB interface

USB Audio Class 1.0 running at Full Speed (12Mbps) is used to deliver processed voice audio to the host processor, stereo reference audio from the host and as a control interface. In this mode the adaptive USB Audio endpoint is used to generate an MCLK synchronised to the USB host. This is driven out of MCLK_INOUT.

The table below shows the signals required to implement a USB interface using the XVF3615.

Table 5.3: USB connections

Name	Description	Pin
USB_DP	Connect to USB connector	29
USB_DM	Connect to USB connector	28
USB_VBUS_DET	Do not connect Self-powered operation is not supported by current device firmware	43
USB_VDD18	1.8V supply for USB-PHY - May be left floating if the USB interface is not used	31
USB_VDD33	3.3V supply to the USB-PHY May be left floating if the USB interface is not used	30

Note: Currently the UA firmware only supports use in a bus powered configuration

5.5 I2S Audio Interface

The XVF3615-INT operates as an I²S Slave outputting audio to the host processor and receiving the reference audio signal. The XVF3615-UA-HYBRID operates as an I²S Master receiving the reference audio signal from the host. The XVF3615-UA and XVF3615-UA-HYBRID may operate as an I²S Master outputting audio for the loudspeakers. The flow of audio samples must be synchronised to a single set of I²S clocks, see table below:

Table 5.4: I²S signals

Signal	Description	Comment	Pin	I/O
MCLK	Master audio clock		14	I
I2S_BCLK	I²S bit synchronisation clock	Configurable for 16kHz (1.024MHz) and 48kHz (3.072MHz) sample rates	13	I
I2S_LRCK	I²S Left/Right clock	48kHz or 16kHz clock derived as I2S_BLCK/64	10	I
I2S_DIN	I²S Data In	Reference audio data from I²S device	53	I
I2S_DOUT	I²S Data Out	Audio data out	9	O

The I²S audio samples are transmitted serially with a one I2S_BCLK delay between the change of I2S_LRCK phase and the start (MSB) of the audio sample for that channel. This the standard alignment for I²S systems.

5.6 I²C Control interface

The I²C Slave interface is used to control and configure the parameters on the XVF3615-INT.

Warning: I²C commands received prior to I²S clocks being activated will not be processed and may result in undefined behaviour. Therefore, it is important to ensure that the I²S interface is activated before parameterisation of the device is undertaken.

The interface operates with the following specifications:

- 100 kbps SCL clock speed
- Register read/write
- Up to 56 byte I²C read/write

For more information on control and configuration of the XVF3615 please refer to the user guide.

The device I²C address is 0x2C, and the pin connections are shown below.

Table 5.5: I²C Slave Connections

Signal	Description	Comment	Pin	I/O
I2C_SCL	I²C serial clock line for receiving control command from I²C host		44	I/O
I2C_SDA	I²C serial data line for receiving control command from I²C host		45	I/O

5.7 General Purpose Input/Output

Four input and four output pins are provided to allow general-purpose I/O such as LEDs and button controls. Input pins can be individually read by the host using the control interface and configured to detect edge events. The output pins can be individually set, and they have configurable Pulse Width Modulated (PWM) brightness control with blinking sequences.

The GPIO pins are shown in the table below.

Table 5.6: GPIO pin table

Name	Description	Pin	I/O
IP_0	General purpose input	46	I
IP_1	General purpose input	50	I
IP_2	General purpose input	48	I
IP_3	General purpose input	51	I
OP_0	General purpose output	40	O
OP_1	General purpose output	54	O
OP_2	General purpose output	55	O
OP_3	General purpose output	56	O

For more information on configuring these inputs and outputs, please refer to the XVF3615 user guide.

6 Device operation

6.1 Power supplies

The XVF3615 has the following power supply pins:

Table 6.1: XVF3615 Power Pins

Name	Description	Pin
VDD	Digital core power supply. 0.9V (nominal)	4 12 19 27 34 42 49 57 61 64
V_DDIOL	Digital I/O power supply ** See Note A	8
V_DDIOR	Digital I/O power supply ** See Note A	38
V_DDIOT	Digital I/O power supply ** See Note A	52
VDD IOB18	Digital I/O power supply. 1.8V (nominal)	17 - 26
PLL_AVDD	PLL analogue power. This 0.9V (nominal) PLL supply should be separated from the other supplies at the same voltage by a low pass filter	22
USB_VDD18	Digital supply to the USB-PHY. 1.8V (nominal)	31
USB_VDD33	Analogue supply to the USB-PHY. 3.3V (nominal)	30
VSS	Device Ground	65 (Paddle)

Warning: A: I/O voltage depends on package variant

- QF60A – VDDIOx is 1.8V nominal – pins 8, 38 and 52 should be connected to a 1.8V supply
- QF60B – VDDIOx is 3.3V nominal – pins 8, 38 and 52 should be connected to a 3.3V supply

For both variants, VDDIOB18 – pins 17 & 26 - must be connected to 1.8V

B: All VDD power pins must be connected.

C: USB_VDDxx supplies can be left floating if USB is not used.

See also:

The XU316-1024-QF60(A/B) datasheets contain further information on power supplies and power on sequencing.

6.2 Clocks

The XVF3615 device has an on-chip oscillator. To use the oscillator a crystal, two capacitors, and damping and feedback resistors to the device as shown below.

Table 6.2: XVF3615 crystal oscillator

Signal	Description	Comment	Pin	I/O
XIN	Crystal oscillator input		16	I
XOUT	Crystal oscillator output		15	O

Fig. 6.1: Crystal oscillator or clock input configurations

Alternatively, the XVF3615 can be provided with a 24MHz, 1V8 clock input on the XIN pin. The clock must be running when the chip comes out of reset.

Table 6.3: XVF3615 clock signals

Signal	Description	Comment	Pin	I/O
XIN	Master clock (system)	24MHz 1V8 clock signal	16	I
XOUT	N/C	Leave floating if clock input on XIN	15	O

See also:

For further information, and details on the calculation of R_f and R_d, please refer to the XU316-1024-QF60(A/B) datasheets.

6.3 Reset

The XVF3615 device has an on-chip Power-on-Reset (POR). This keeps the chip in reset whilst the supplies are coming up.

See XU316-1024-QF60(A/B) datasheet for further information.

Table 6.4: Reset Signal

Signal	Description	Comment	Pin	I/O
RST_N	Device reset	Active low	21	I

6.4 Boot modes

On start-up and after a reset event, the XVF3615 is booted either using an externally connected QSPI flash memory or by transferring a boot image to the device via SPI from a host processor.

6.4.1 Slave boot mode

The boot mode is specified using QSPI_D1/BOOTSEL. If this pin is tied high via a 4.7k ohm resistor on start-up, the XVF3615 will enable SPI Slave boot mode and activate the pins shown below.

Table 6.5: SPI Slave boot pins

Signal	Description	Comment	Pin	I/O
QSPI_CLK / SPI_CLK	SPI Clock		5	I
SPI_CS_N	SPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	6	I
SPI_MOSI	SPI Master Out Slave In		7	I
SPI_MISO	SPI Master In Slave Out		47	O

6.4.2 QSPI Master boot mode

If the QSPI_D1/BOOTSEL pin is connected to a QSPI_D1 pin on a flash device, the XVF3615 will boot from a local QSPI flash in QSPI Master mode. The active pins are shown below.

Table 6.6: QSPI Master peripheral interface pins

Name	Description	Pin	I/O
QSPI_CS_N	QSPI Chip Select. This pin should be pulled high externally to the device using a 4.7k ohm resistor	3	I/O
QSPI_D0	QSPI Data Line 0	59	I/O
QSPI_D1 - BOOTSEL	QSPI Data Line 1 and boot selection. To activate QSPI Master boot mode connect directly to QSPI Data Line 1 on Quad capable flash device	1	I/O
QSPI_D2	QSPI Data Line 2	60	I/O
QSPI_D3	QSPI Data Line 3	2	I/O
QSPI_CLK / SPI_CLK	QSPI Clock and SPI Clock	5	I/O

6.5 QSPI flash support

Flash devices with the following specifications are supported by the XVF3615 (e.g. Winbond W25Q16JWSNIM).

Table 6.7: Flash device specification supported by XVF3615

Device characteristic	Description	Value
Page size	Size of flash page in bytes	256
Number of pages	Total number of pages	8192
Address size	Number of bytes used to represent the address	3
Read ID operation code	Operation code to read the device identification (ID) information	0x9F
Read ID dummy bytes	Number of dummy bytes after read command before ID is returned	0
ID size	Size of ID in bytes	3
Sector Erase operation code	Operation code for 4kB Erase	0x20
Sector information	Arrangement of sectors	Regular (all equally sized - 4kB)
Write Enable operation code	Operation code for write enable	0x06
Write Disable operation code	Operation code for write disable	0x04
Page Program operation code	Operation code for page program	0x02
Fast Quad Read operation code	Operation code for Fast Quad I/O Read	0xEB
Fast Quad Read Dummy Bytes	Number of dummy bytes after setup of fast quad read that data is returned	1
Read Status Register operation code	Operation code for reading status register	0x05
Write Status Register operation code	Operation code for write to the status register	0x01
Write Status Register Busy Mask	Bit mask for operation in progress (device busy)	0x01

6.6 Device firmware

Device Firmware Upgrade (DFU) is supported for devices that have QSPI flash connected and loaded with a firmware image. If the DFU process fails, the boot process safely falls back to the factory image allowing the user to re-attempt the upgrade. Images loaded via DFU can also be removed allowing the device to revert to the factory image.

For further information on the operation of the DFU mechanism refer to the *Upgrade Images and Data Partitions* section of the XVF3615 user guide.

7 Device characteristics

7.1 Electrical and Thermal characteristics

For electrical and thermal characteristics, including Absolute Maximum ratings please refer to the XU316-1024-QF60(A/B) datasheets.

xcore.ai base datasheet links:

XU316-1024-QF60A

XU316-1024-QF60B

8 Switching characteristics

For clock, reset and JTAG timing refer to the XU316-1024-QF60(A/B) datasheet. XVF3615 specific interface timings are detailed below.

8.1 QSPI Master (External flash for boot image storage)

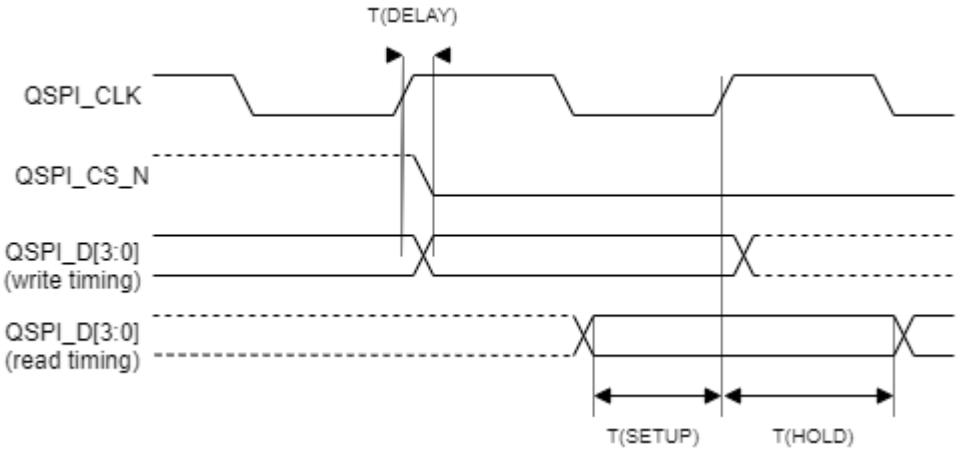


Fig. 8.1: QSPI Timing

Table 8.1: QSPI Timing Requirements

Parameter	Symbol	Min	Typical	Max	Units
QSPI Clock frequency	f(QSPI_CLK)	-	15.6	-	MHz
QSPI_CLK to QSPI Data output delay	T(DELAY)	-2.7	-	2.7	ns
QSPI Data input to QSPI_CLK Setup time	T(SETUP)	22	-	-	ns
QSPI Data input to QSPI_CLK hold time	T(HOLD)	-11	-	-	ns

8.2 I2S Slave

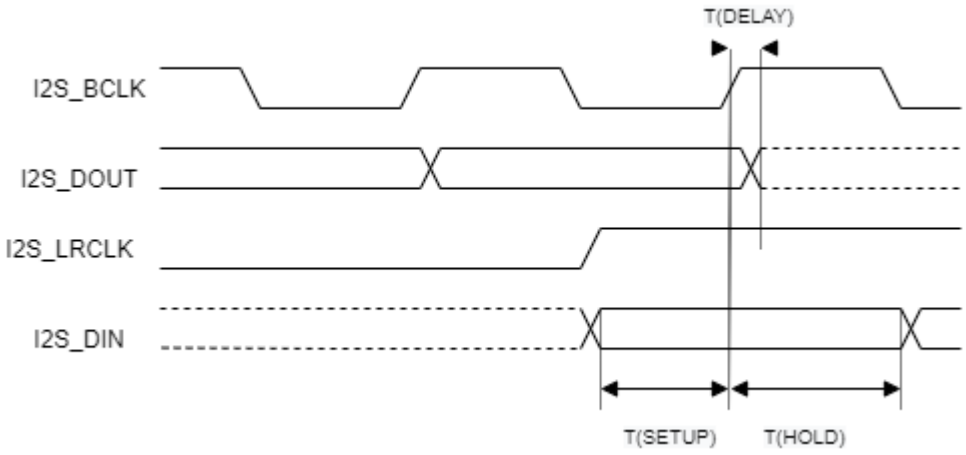


Fig. 8.2: I²S Slave timing

Table 8.2: I²S Slave Timing Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Master clock input frequency	f(MCLKin)	-	12.288	24.576	MHz	A
I2S Bit Clock frequency input	f(I2S_BCLK)	1.024	-	3.072	MHz	
I2S Data Input (LRCLK) to I2S_BCLK setup time	T(SETUP)	0	-	-	ns	B
I2S Data Input (LRCLK) to I2S_BCLK hold time	T(HOLD)	6	-	-	ns	B
I2S_BCLK to I²S Data output delay	T(DELAY)	11	-	21.3	ns	

A: Configurable input multiplier used to generate appropriate audio sample rates (16kHz / 48kHz)

B: Timing also applies to I²S Sample Clock (I2S_LRCLK)

8.3 SPI Slave (External processor boot)

Table 8.3: SPI Slave Timing Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
SPI Clock frequency	f(SPI_CLK)	-	12.5	-	MHz	
SPI_CLK to MISO output delay	T(DELAY)	11	-	21.3	ns	
SPI Master Output Slave Input (MOSI) to SPI_CLK Setup time	T(SETUP)	0	-	-	ns	
SPI Master Output Slave Input to (MOSI) SPI_CLK hold time	T(HOLD)	6	-	-	ns	

A: Timing also applies to SPI Chip Select input (SPI_CS_N)

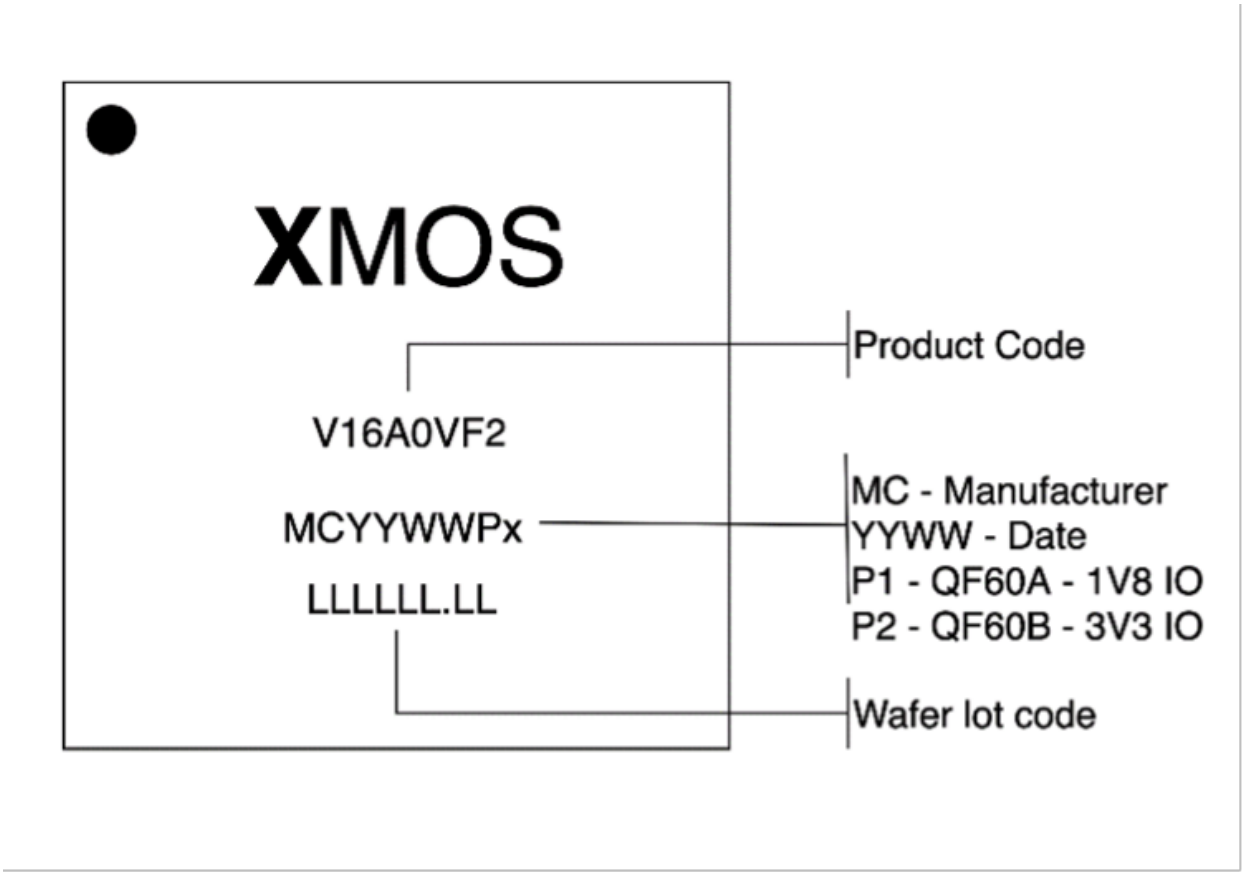
8.4 SPI Master (Peripheral control)

Table 8.4: SPI MasterTiming Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
SPI Clock frequency	f(SCLK)	-	1.0	-	MHz	
SPI CLK to SPI Master In Slave Out (MOSI) output delay	T(DELAY)	-2.7	-	2.7	ns	
SPI Master Out Slave In (MISO) Setup time	T(SETUP)	0	-	-	ns	
SPI Master Out Slave In (MISO) Hold time	T(HOLD)	6	-	-	ns	

9 Package information

9.1 Device markings



Important: The picture above represents the commercial package, the industrial package is distinguished by an *I* after the product code, i.e. V16A0VF2I.

Important: The two variants of the package (1.8V and 3.3V I/O) are distinguished by a *P1* or *P2* code after the date code (*YYWW*) on the package

9.2 Order codes

Table 9.1: Ordering codes

Product code	Marking **	Description
XVF3615-QF60A-C	V16A0VF2 MCYYWWP1	Commercial Temp range (0 – 70 degrees Celsius) - 1.8V IO
XVF3615-QF60B-C	V16A0VF2 MCYYWWP2	Commercial Temp range (0 – 70 degrees Celsius) - 3.3V IO
XVF3615-QF60A-I	V16A0VF2I MCYYWWP1	Industrial Temp range (40 – 85 degrees Celsius) - 1.8V IO
XVF3615-QF60B-I	V16A0VF2I MCYYWWP2	Industrial Temp range (40 – 85 degrees Celsius)) - 3.3V IO

Note: ** MC – Manufacturer, YY – Year code, WW – Week code, Px - I/O volage

9.3 Moisture Sensitivity Level

The package moisture sensitivity level rating is MSL-3. Devices have a shelf life of 168 hours between removal from the packaging and reflow, provided they are stored below 30C and 60% RH. If devices have exceeded these values or an included moisture indicator card shows excessive levels of moisture, then the parts should be baked as appropriate before use. This is based on information from Joint IPC/JEDEC Standard for Moisture/Reflow Sensitivity Classification for Non-hermetic Solid-State Surface-Mount Devices (J-STD-020 Revision D).

9.4 Hazardous Materials

This product complies with the Reduction of Hazardous Substances (RoHS) directive.

For details refer to https://www.xmos.com/environmental.