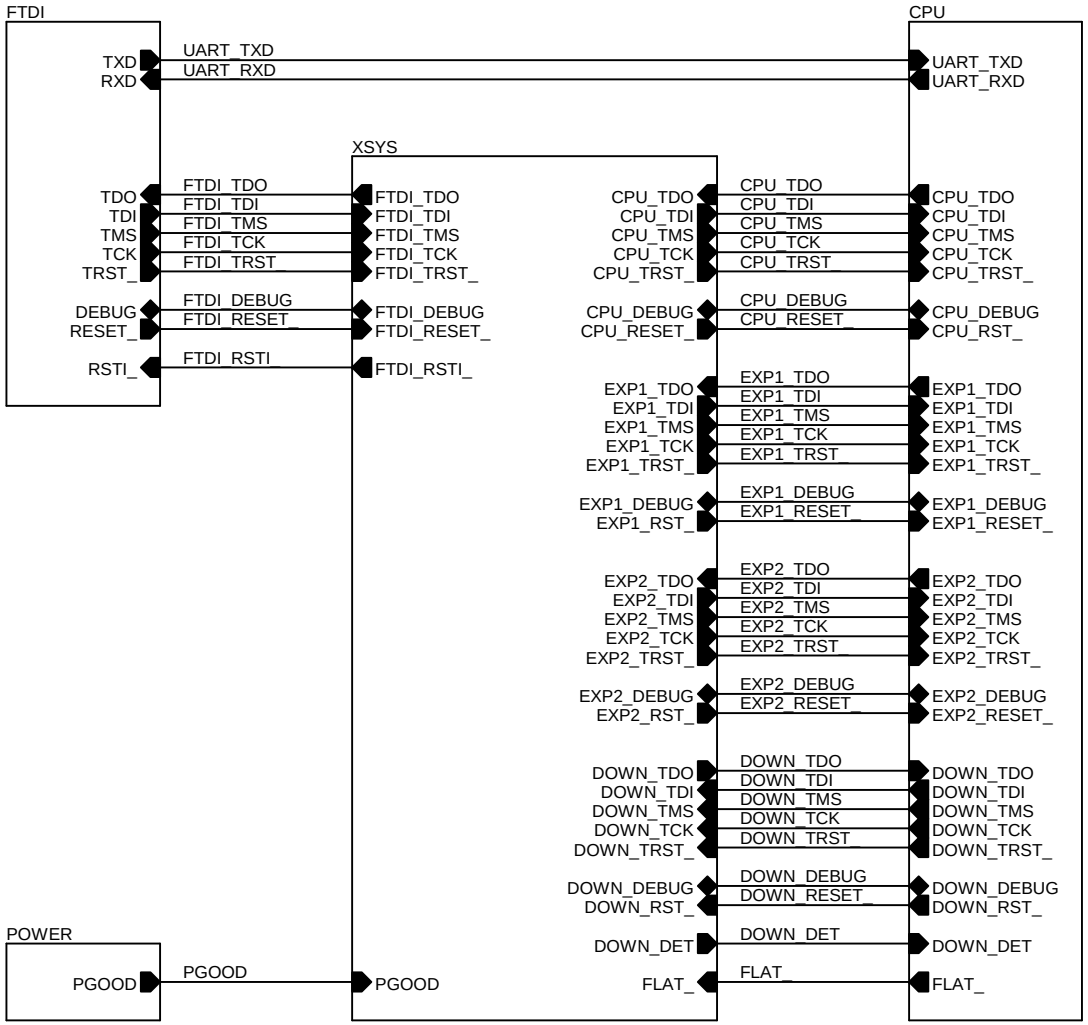
04/07/2008 XDK-M1_2-1_5.DSN VARIANTS A & B (CPU REV)
24/07/2008 XDK-M1_2-1_5_MOD1.DSN MOD1 DETAILS

MODIFICATIONS:

MOD1 X1D39/X1E39 CONNECTIONS TO U16



MISC1 PCB XDK-M1 REV 2.1

Schematic: ROOT	
Title: XMOS XDK-M1	
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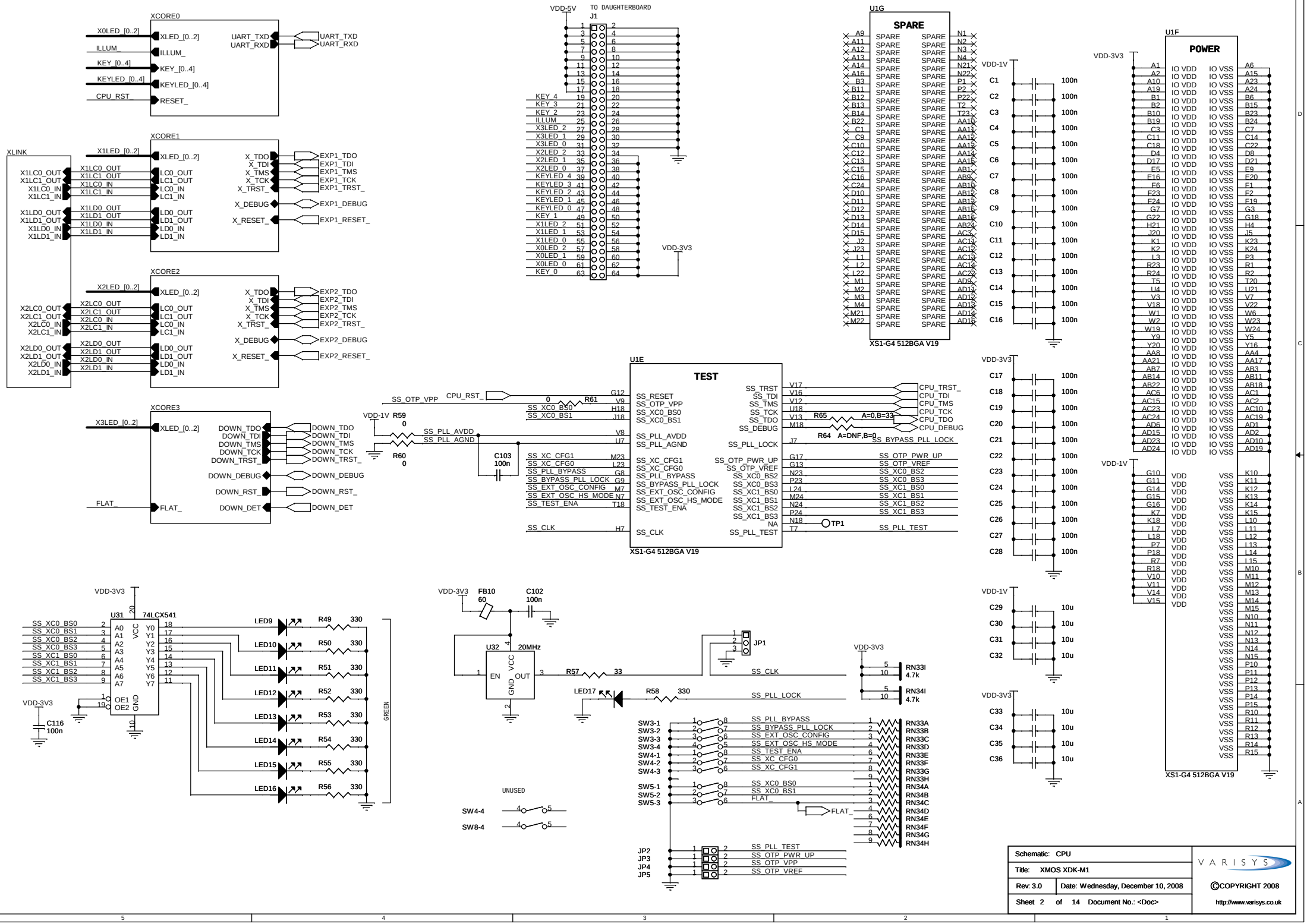
XCORE0
XCORE1
XCORE2
XCORE3
XLINK
TO DAUGHTERBOARD
J1
U1G
SPARE
XS1-G4 512BGA V19
U1F
POWER
U1E
TEST
U31
74LCX541
U32
20MHz
JP1
UNUSED
SW4-4
SW8-4
Schematic: CPU
Title: XMOS XDK-M1
Rev: 3.0
Date: Wednesday, December 10, 2008
Sheet 2 of 14
Document No.: <Doc>
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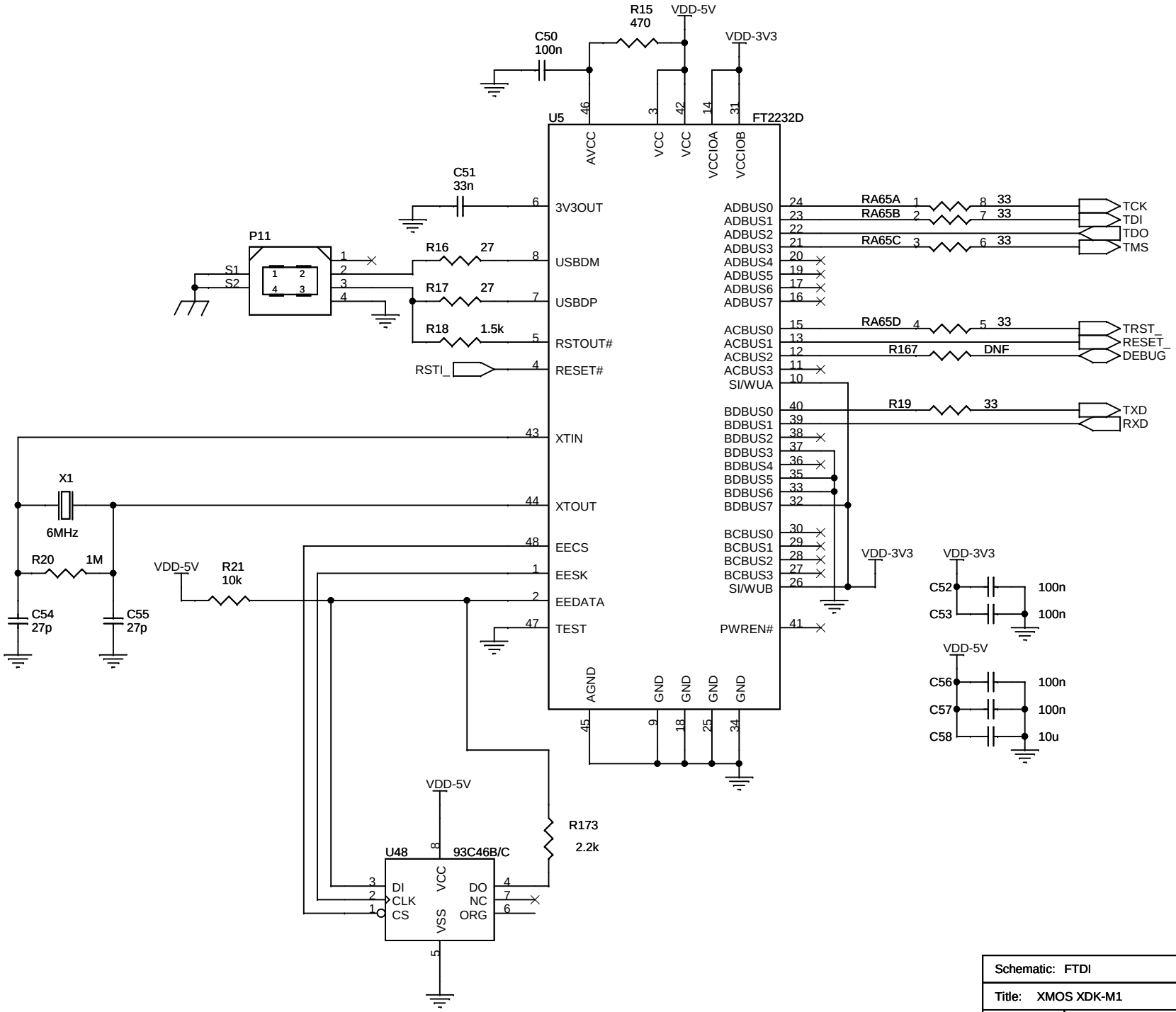
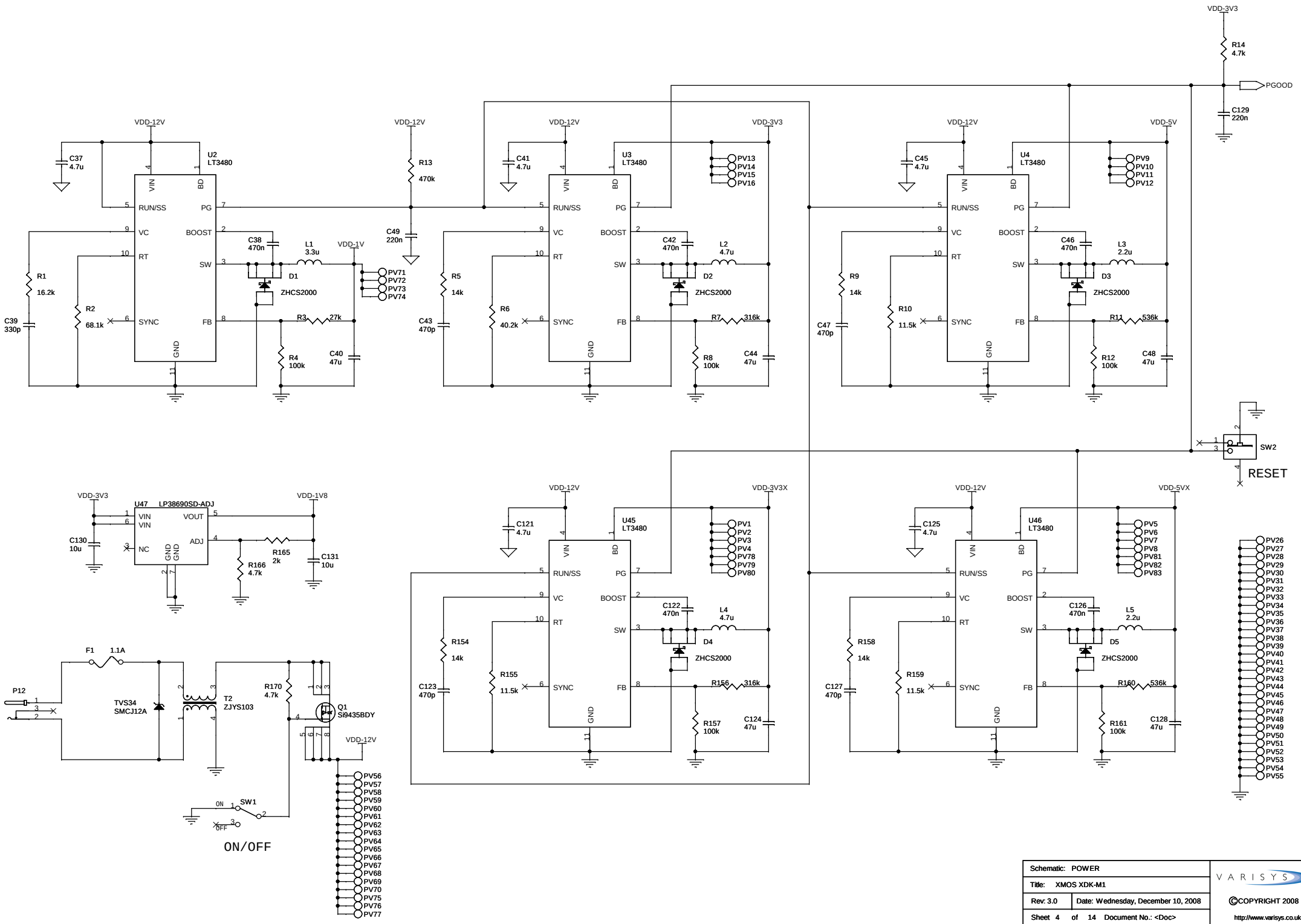
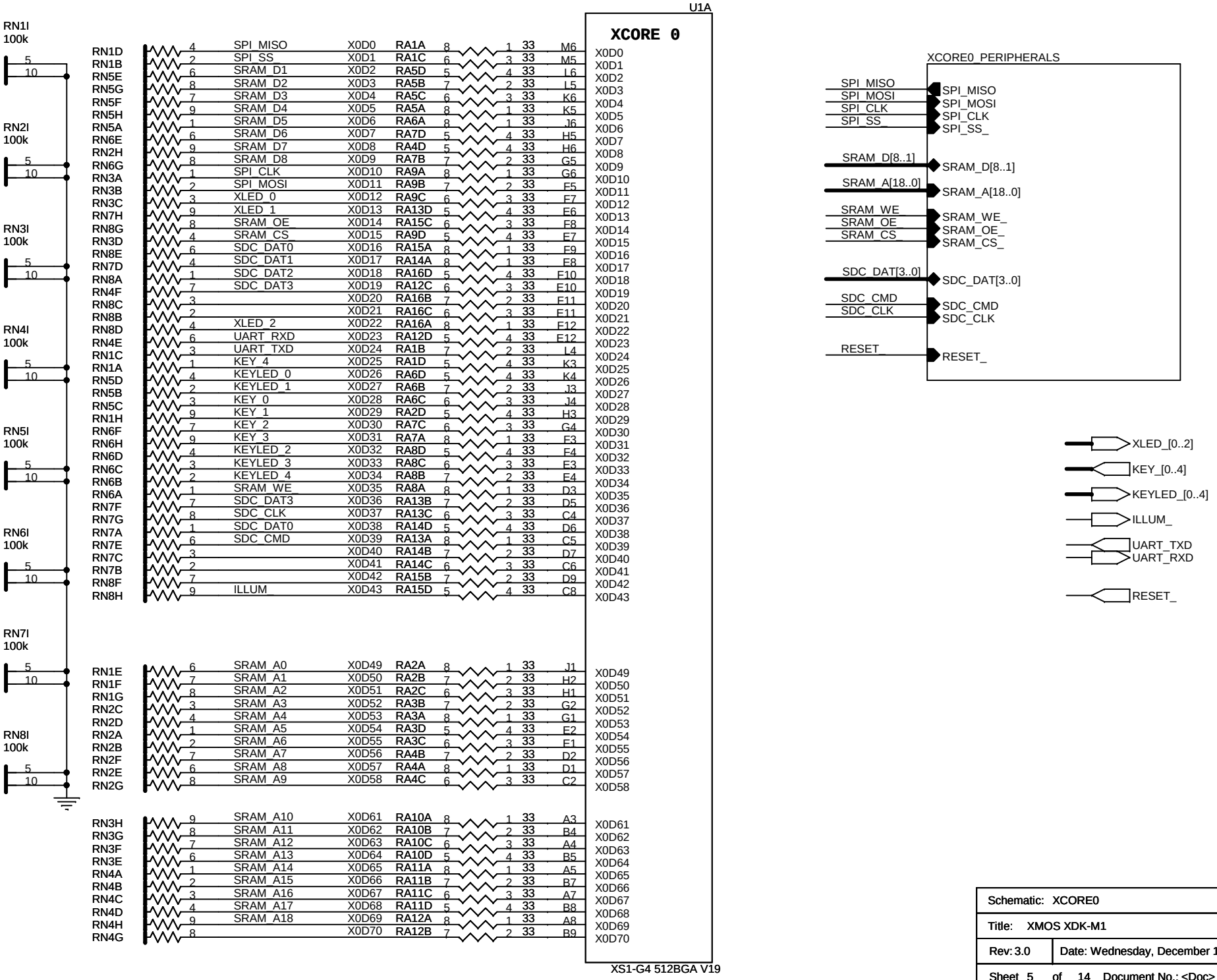


Schematic: FTDI		VARISYS
Title: XMOS XDK-M1		
Rev: 3.0	Date: Wednesday, December 10, 2008	©COPYRIGHT 2008
Sheet 3 of 14	Document No.: <Doc>	http://www.varisys.co.uk



Schematic: POWER	
Title: XMOS XDK-M1	
Rev: 3.0	Date: Wednesday, December 10, 2008
Sheet 4 of 14	Document No.: <Doc>



Schematic: XCORE0	
Title: XMOS XDK-M1	
Rev: 3.0	Date: Wednesday, December 10, 2008
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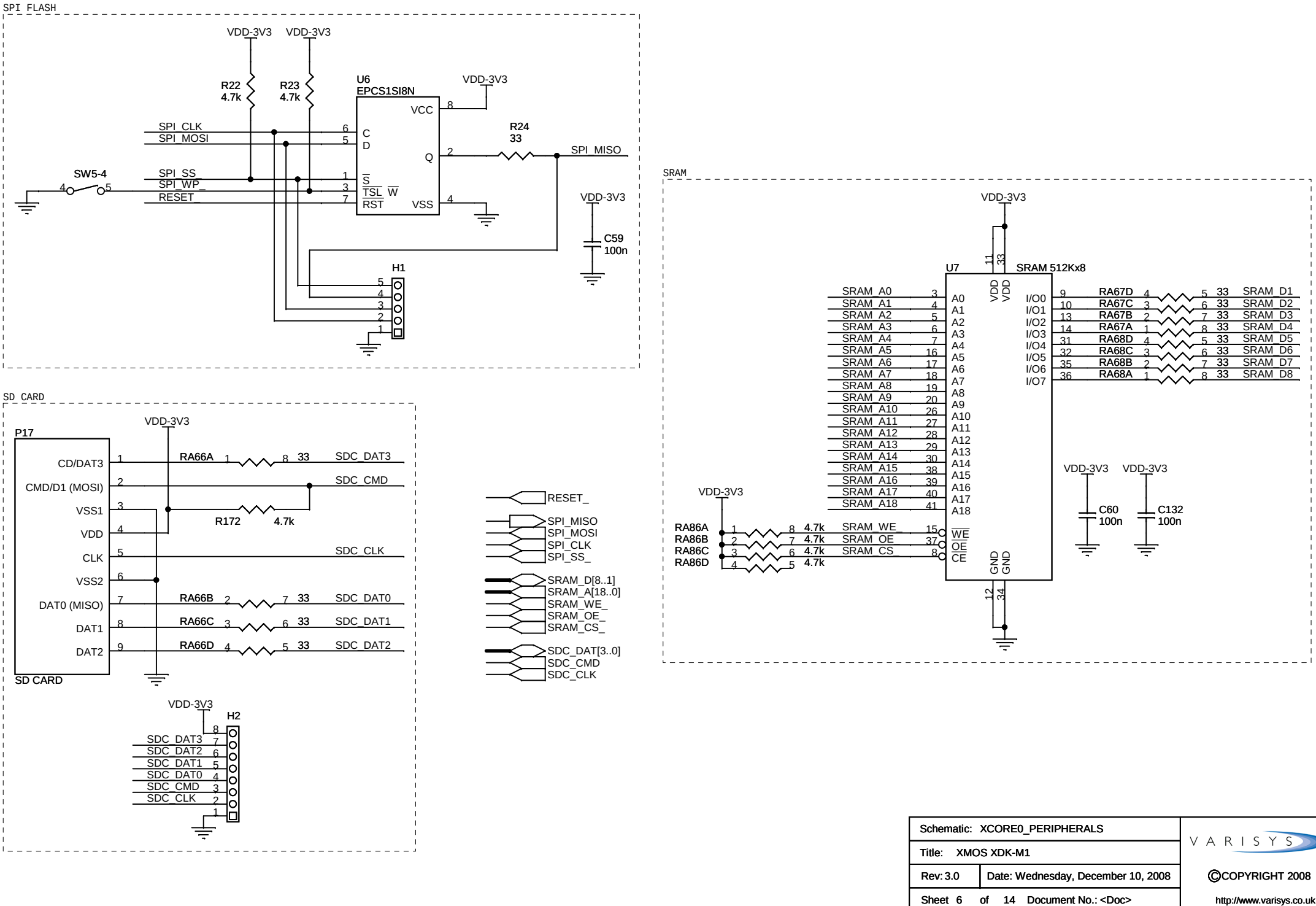
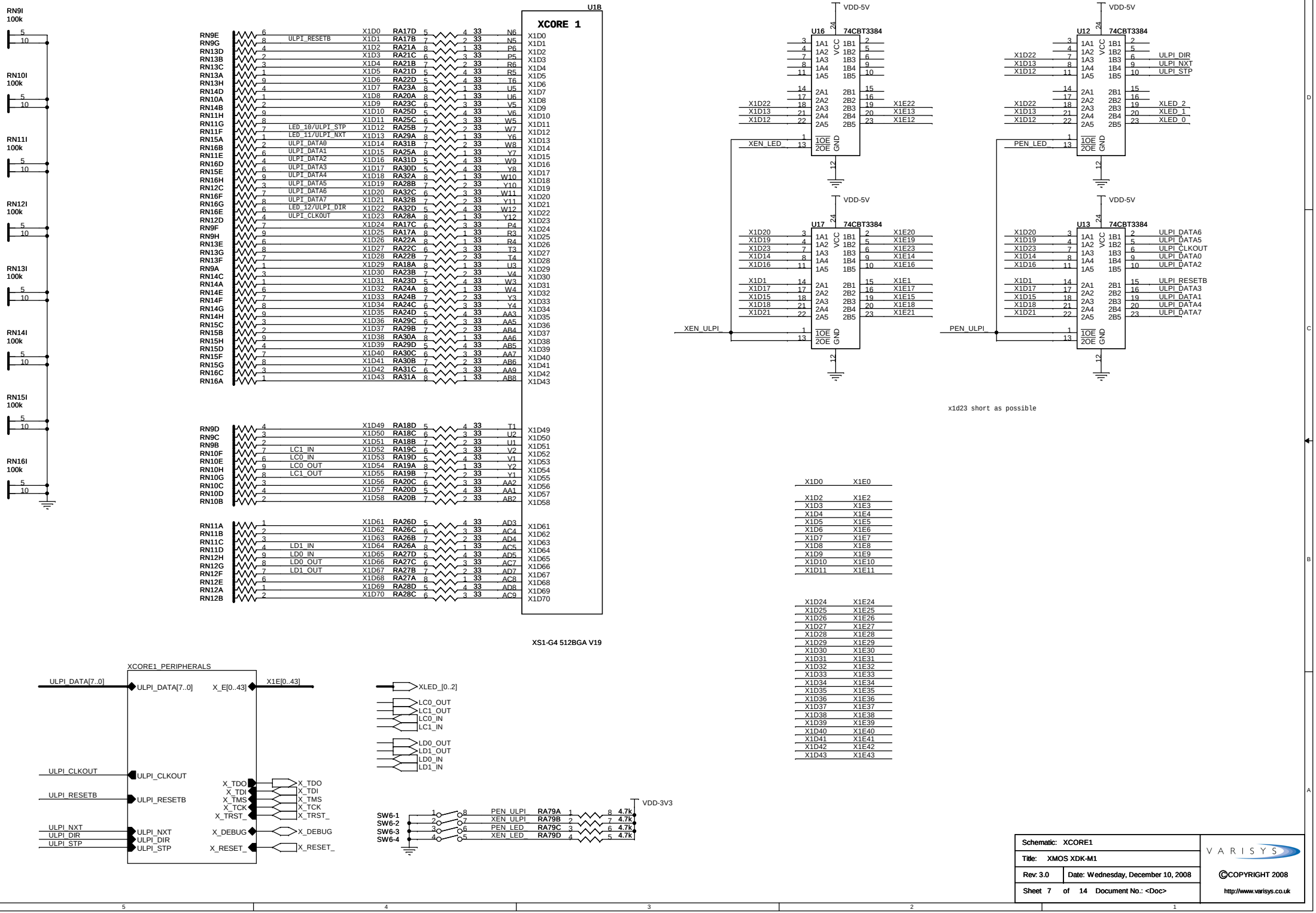


Schematic: XCORE0_PERIPHERALS		VARISYS
Title: XMOS XDK-M1		©COPYRIGHT 2008
Rev: 3.0	Date: Wednesday, December 10, 2008	
Sheet 6 of 14	Document No.: <Doc>	http://www.varisys.co.uk



X1D0	X1E0
X1D2	X1E2
X1D3	X1E3
X1D4	X1E4
X1D5	X1E5
X1D6	X1E6
X1D7	X1E7
X1D8	X1E8
X1D9	X1E9
X1D10	X1E10
X1D11	X1E11

X1D24	X1E24
X1D25	X1E25
X1D26	X1E26
X1D27	X1E27
X1D28	X1E28
X1D29	X1E29
X1D30	X1E30
X1D31	X1E31
X1D32	X1E32
X1D33	X1E33
X1D34	X1E34
X1D35	X1E35
X1D36	X1E36
X1D37	X1E37
X1D38	X1E38
X1D39	X1E39
X1D40	X1E40
X1D41	X1E41
X1D42	X1E42
X1D43	X1E43

Schematic:	XCORE1
Title:	XMOS XDK-M1
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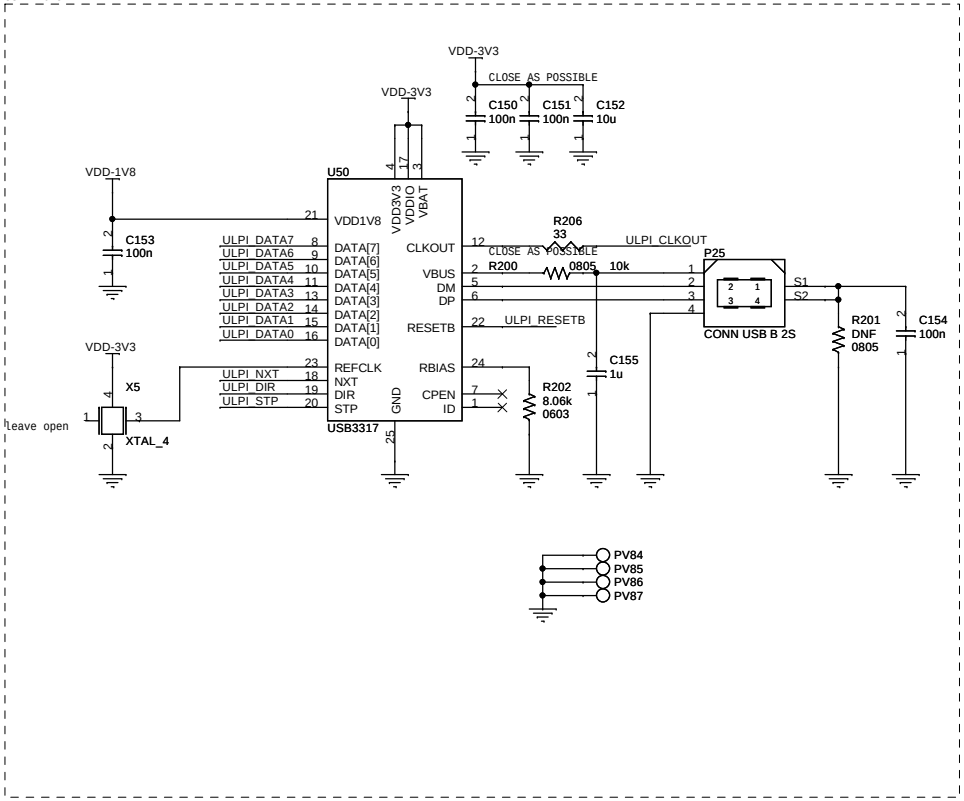
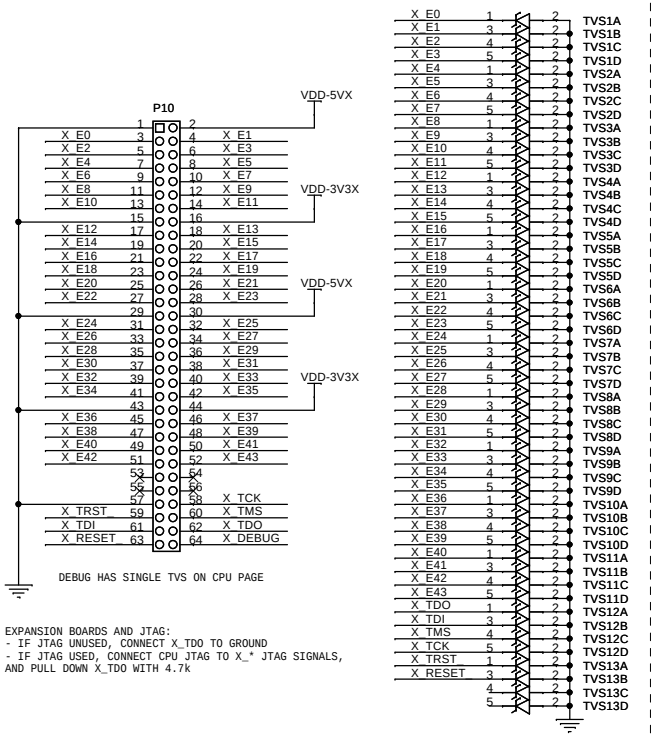
USB 2.0 UTMI PHY



XIO IDC CONNECTOR



DEBUG HAS SINGLE TVS ON CPU PAGE

EXPANSION BOARDS AND JTAG:
- IF JTAG UNUSED, CONNECT X_TDO TO GROUND
- IF JTAG USED, CONNECT CPU JTAG TO X_* JTAG SIGNALS, AND PULL DOWN X_TDO WITH 4.7k

X_E[0..43]
X_TDO
X_TDI
X_TMS
X_TCK
X_TRST_
X_DEBUG
X_RESET_
ULPI_DATA[7..0]
ULPI_NXT
ULPI_DIR
ULPI_STP
ULPI_CLKOUT
ULPI_RESETB

Schematic: XCORE1_PERIPHERALS	
Title: XMOS XDK-M1	
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Sheet 8 of 14	Document No.: <Doc>

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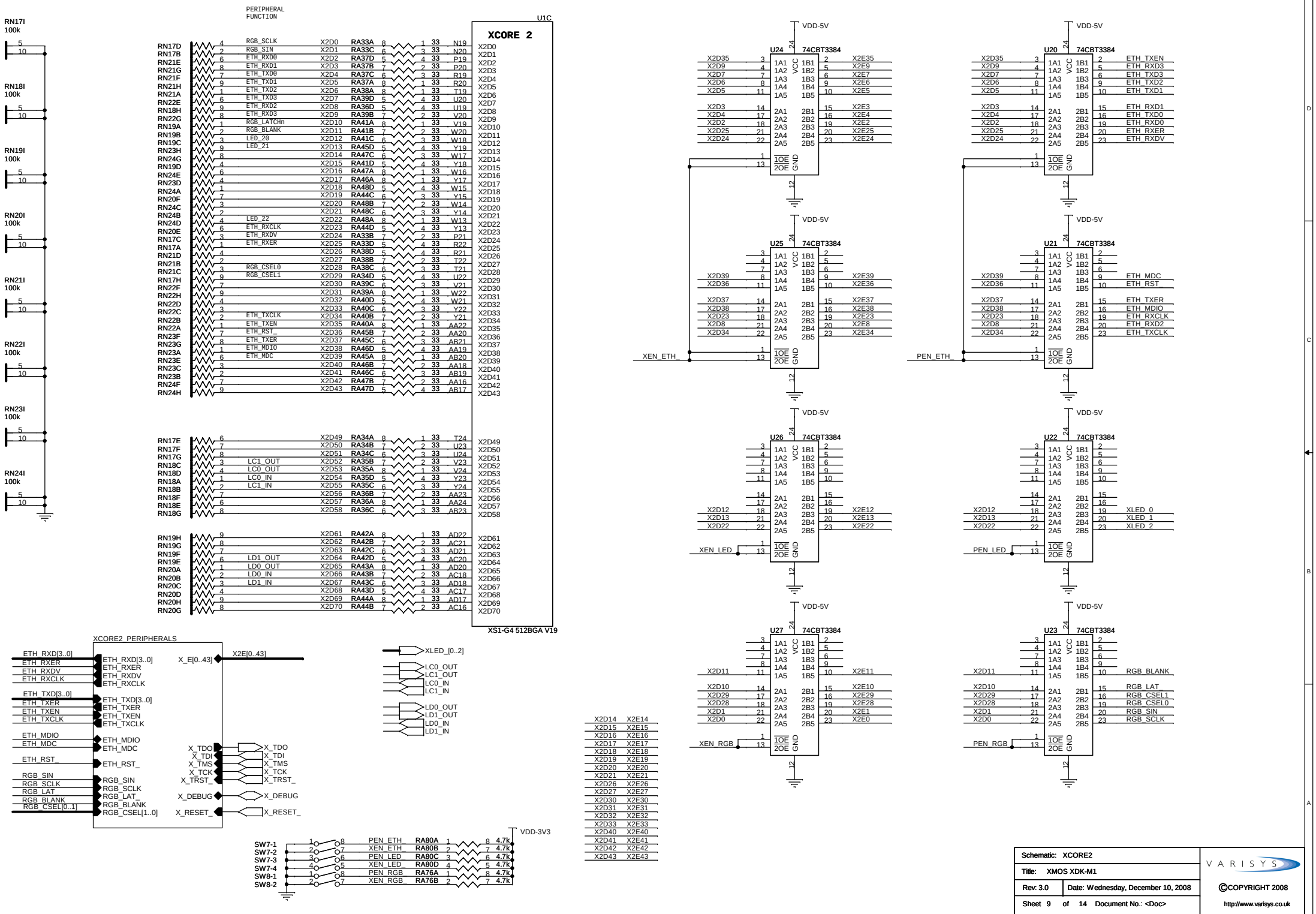

Schematic: XCORE2	
Title: XMOS XDK-M1	
Rev: 3.0	Date: Wednesday, December 10, 2008
Sheet 9 of 14	Document No.: <Doc>

VARISYS

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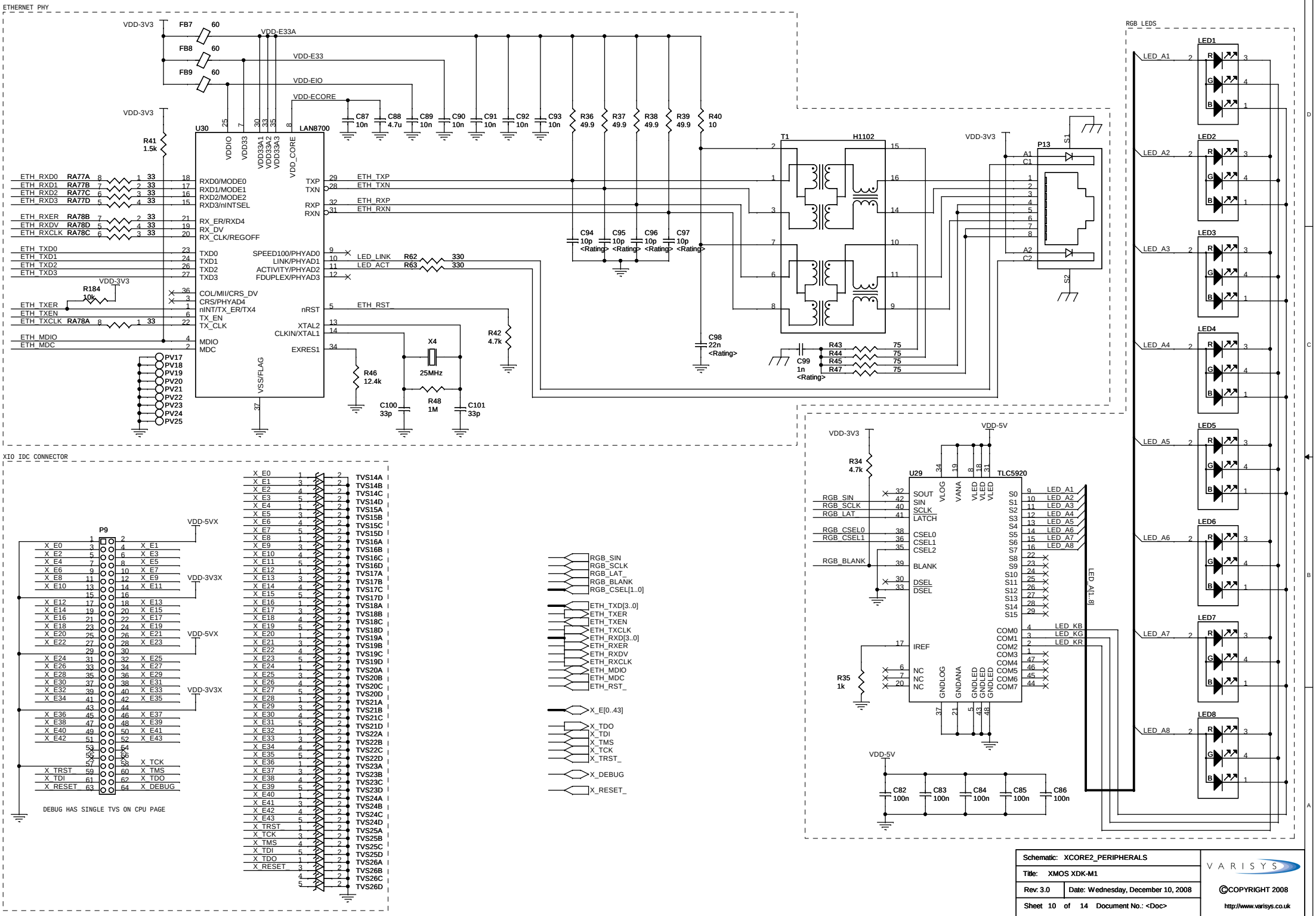
ETHERNET PHY
XIO IDC CONNECTOR
RGB_LEDS
U30
LAN8700
T1
H1102
P13
P9
U29
TLC5920
DEBUG HAS SINGLE TVS ON CPU PAGE
Schematic: XCORE2_PERIPHERALS
Title: XMOS XDK-M1
Rev: 3.0
Date: Wednesday, December 10, 2008
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Document No.: <Doc>
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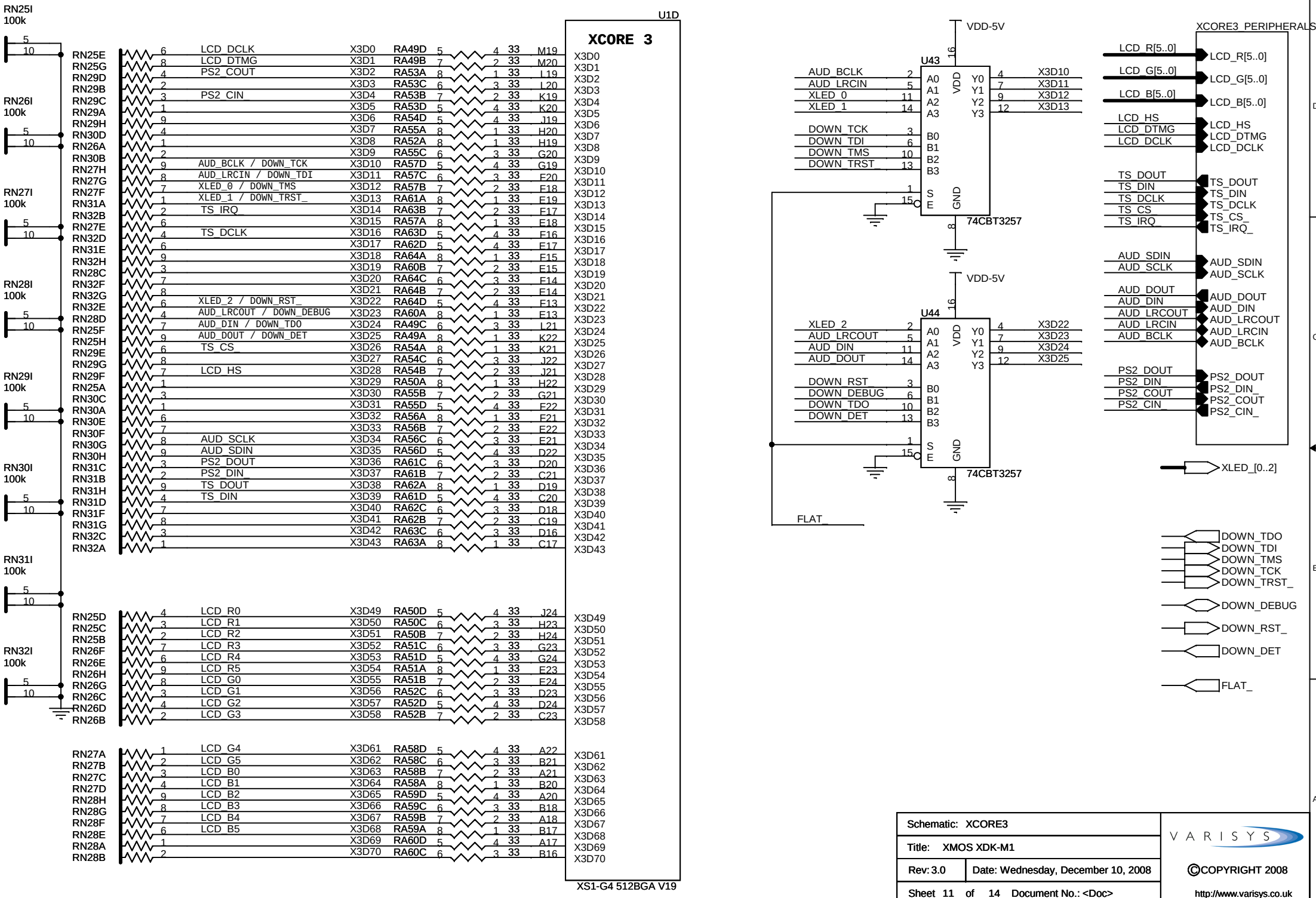

Schematic: XCORE3	VARISYS
Title: XMOS XDK-M1	
Rev: 3.0	Date: Wednesday, December 10, 2008
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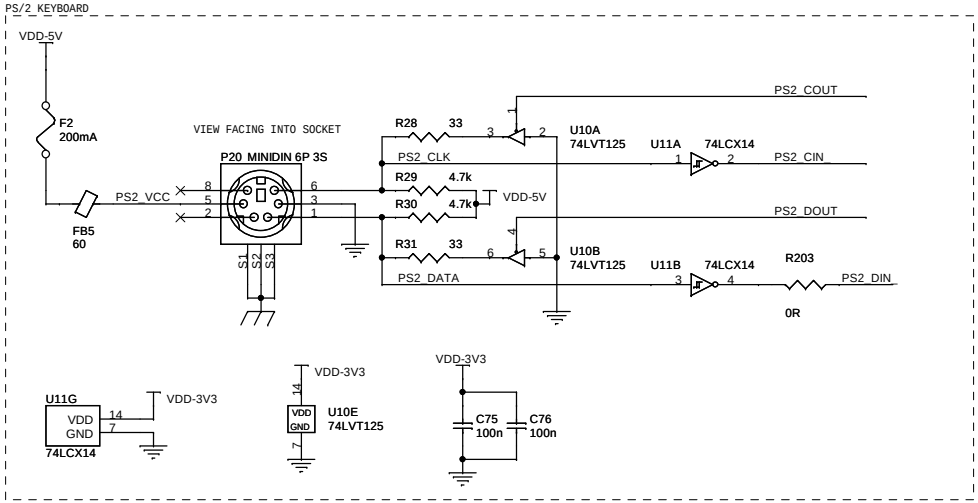
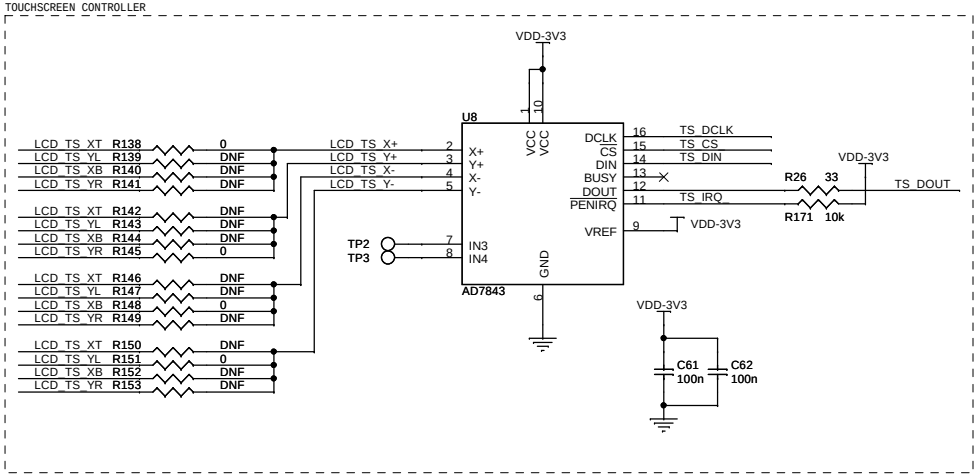
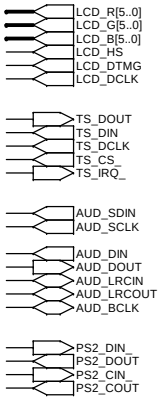
PS/2_KEYBOARD

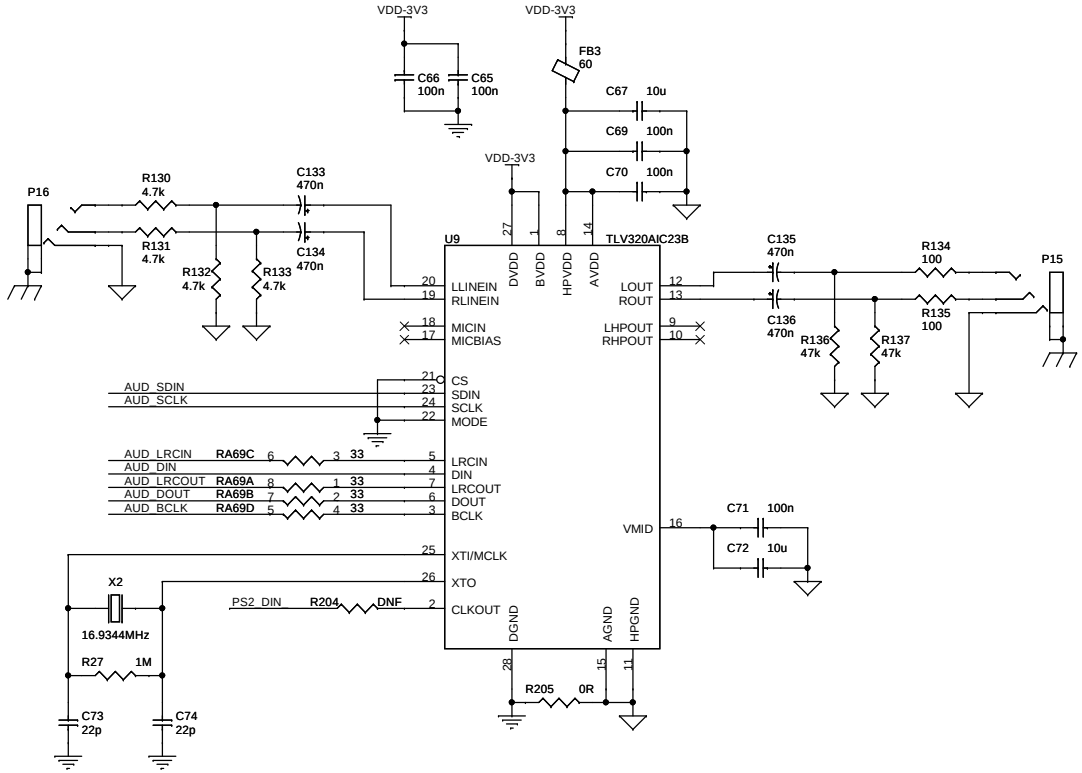


TOUCHSCREEN CONTROLLER

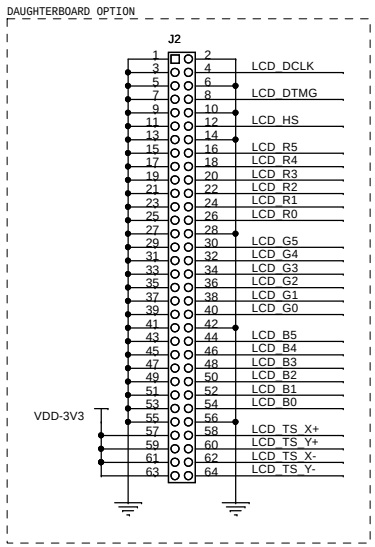




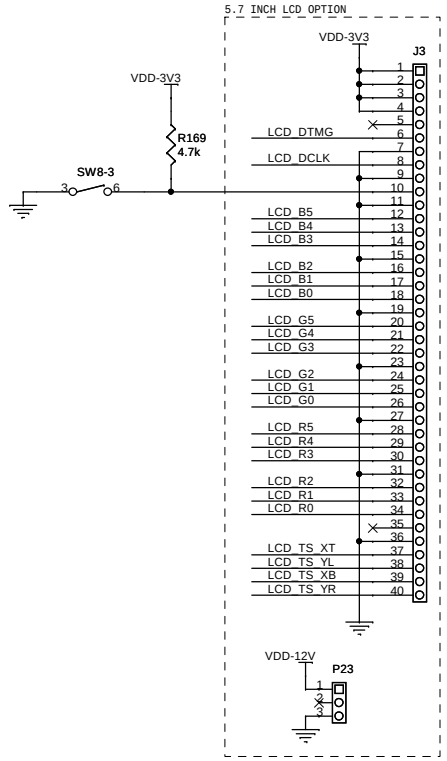
AUDIO CODEC



DAUGHTERBOARD OPTION



5.7 INCH LCD OPTION



Schematic: XCORE3_PERIPHERALS		VARISYS
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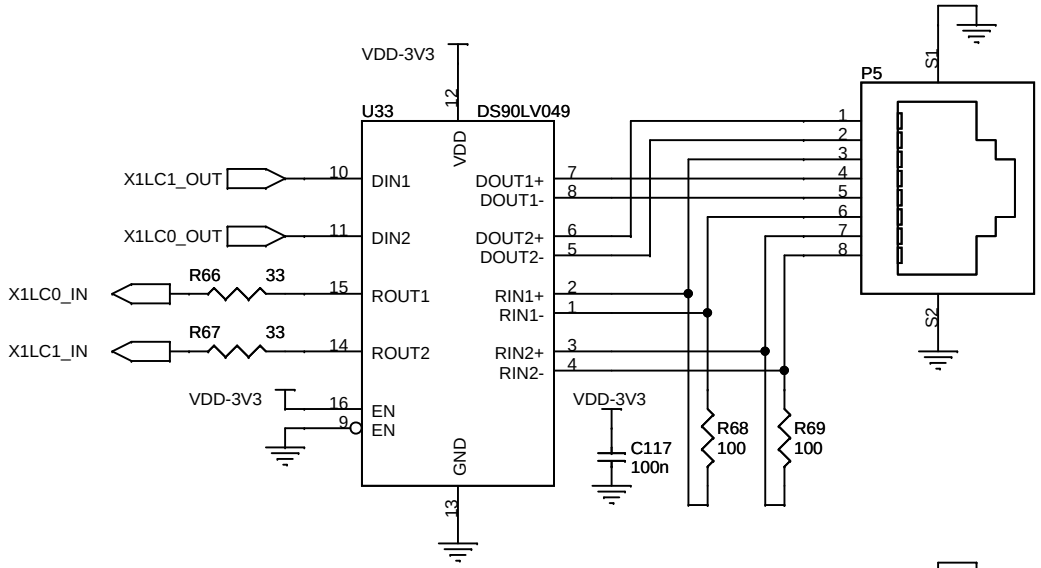
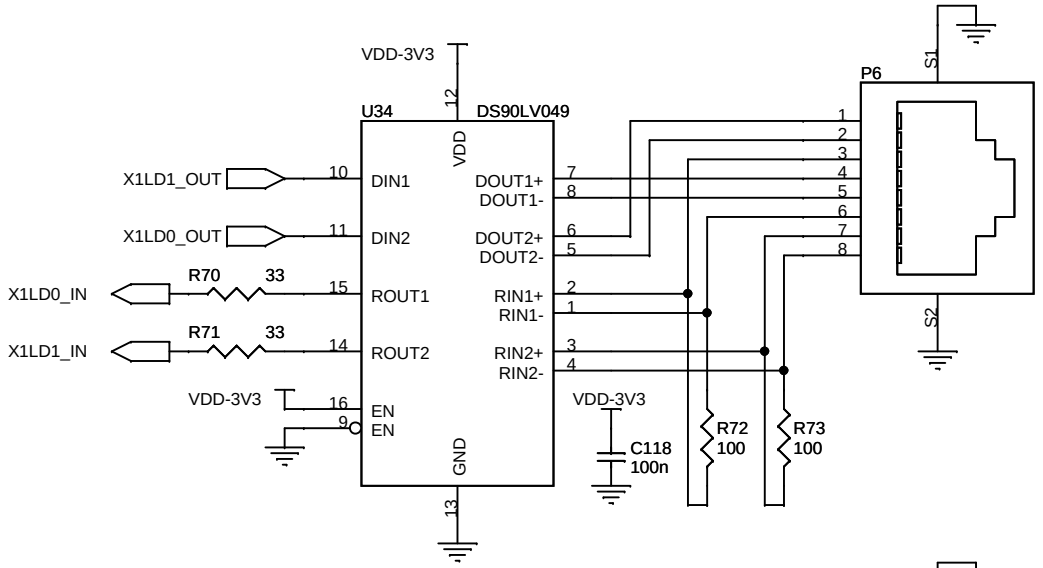
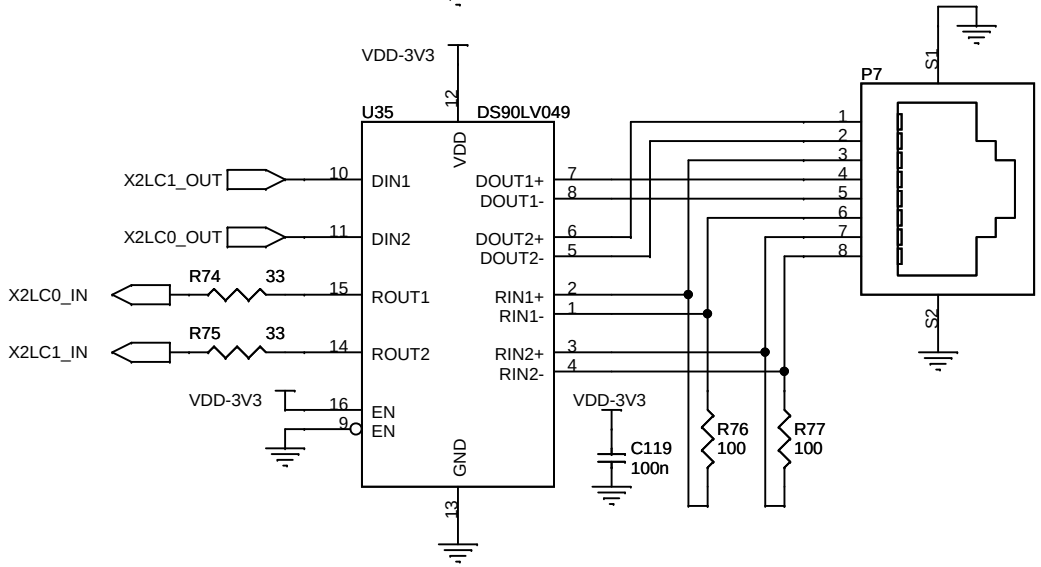
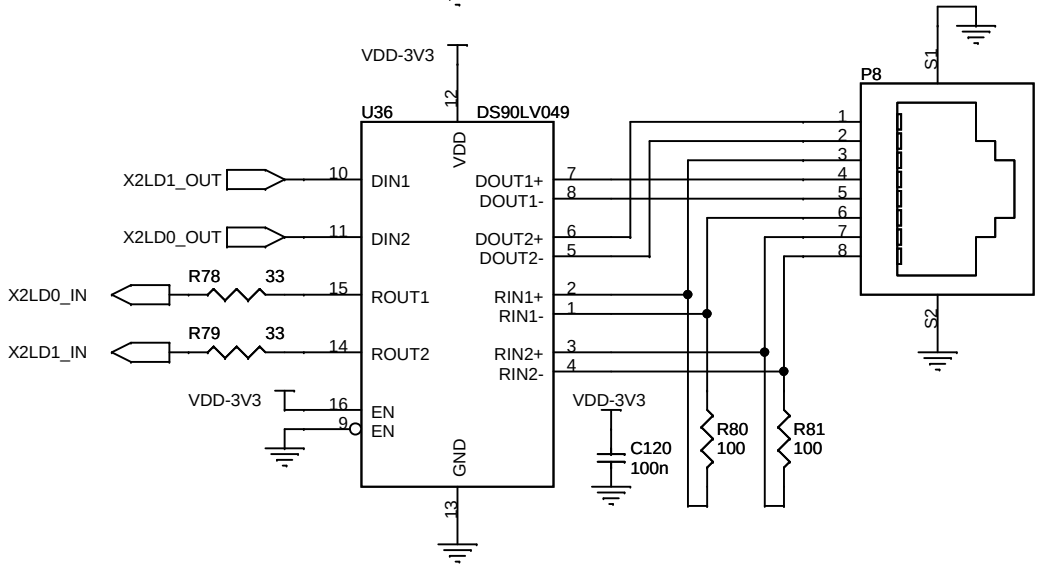




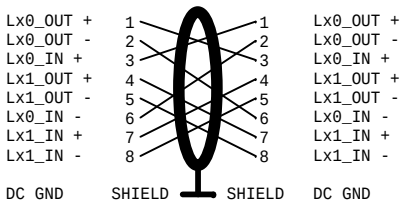




RJ45 PINOUT:

1/2	Lx0_OUT +/-
3/6	Lx0_IN +/-
4/5	Lx1_OUT +/-
7/8	Lx1_IN +/-

CAT 5e / CAT 6 CROSS WIRED STP PATCH CABLE



Schematic: XLINK		VARISYS
Title: XMOS XDK-M1		
Rev: 3.0	Date: Wednesday, December 10, 2008	©COPYRIGHT 2008
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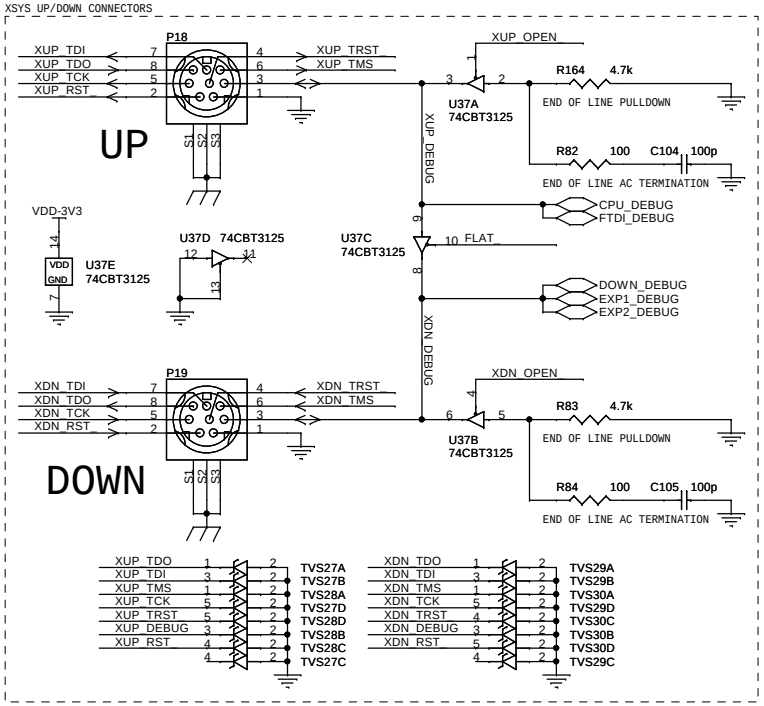
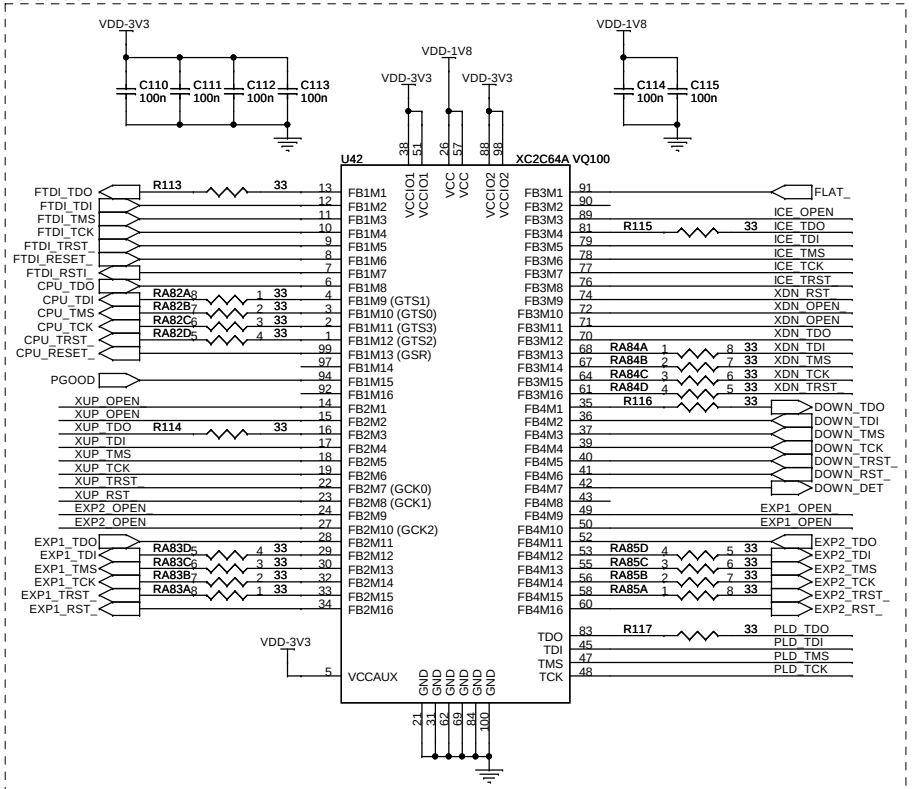
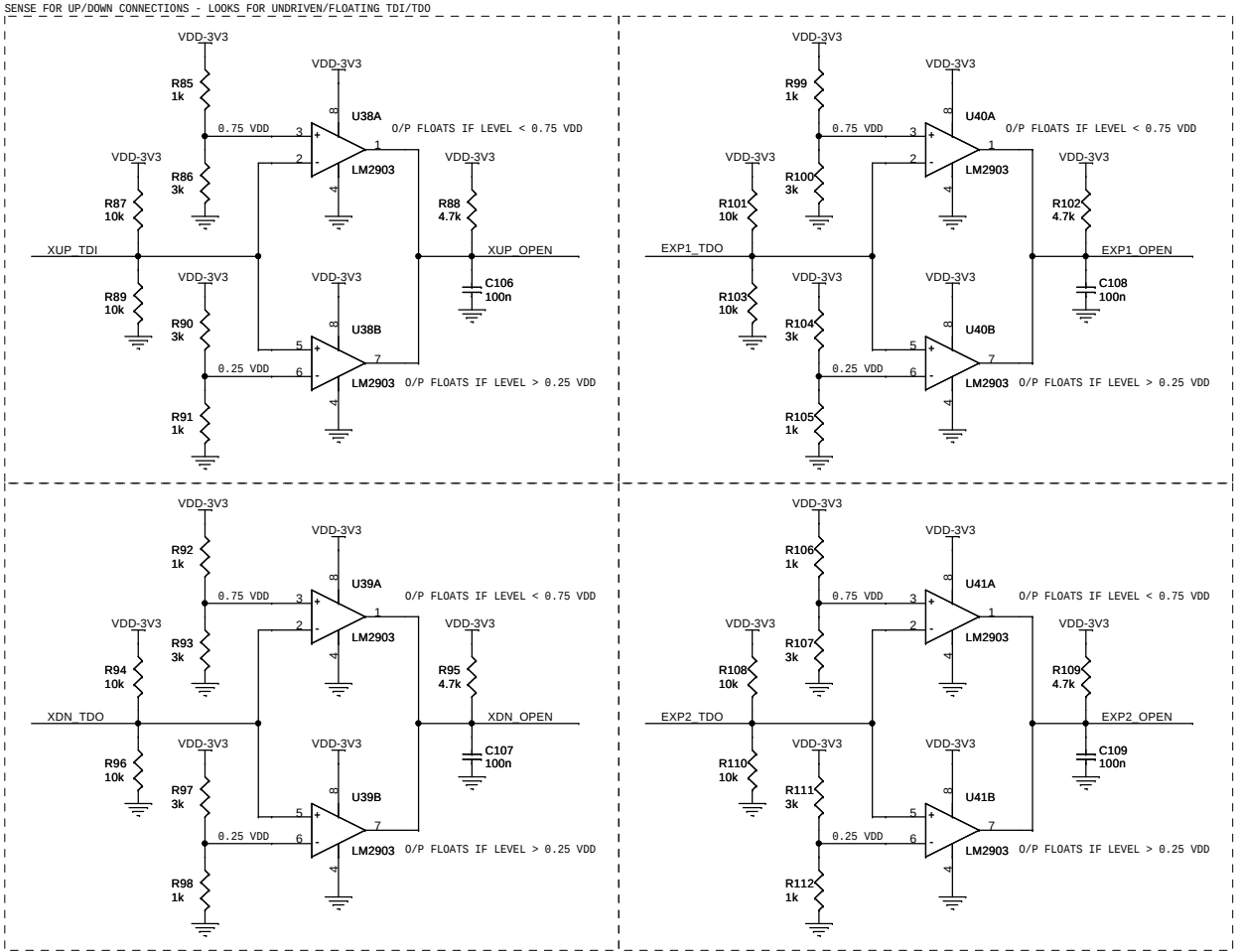
XSYS UP/DOWN CONNECTORS



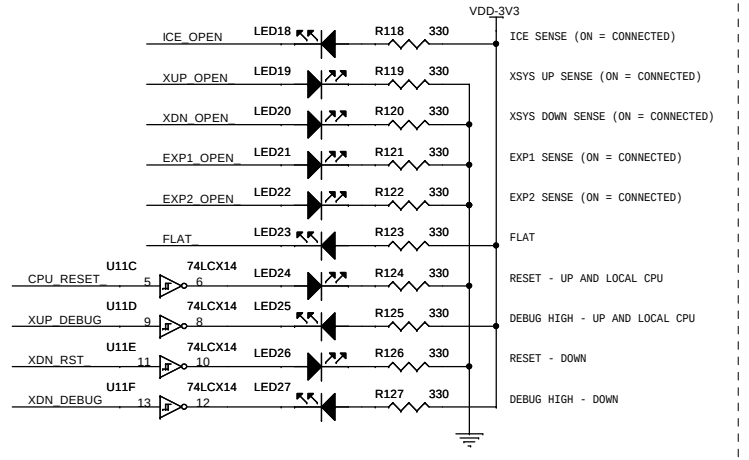
RESET/JTAG STEERING



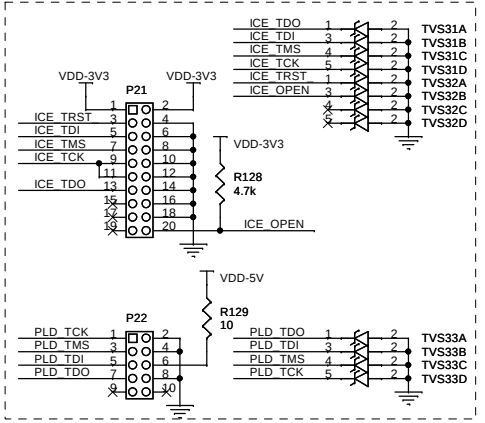
SENSE FOR UP/DOWN CONNECTIONS - LOOKS FOR UNDRIVEN/FLOATING TDI/TDO



XSYS STATUS LEDS (YELLOW)



IN CIRCUIT EMULATOR AND PLD PROGRAMMING HEADERS



Schematic: XSYS	VARISYS
Title: XMOS XDK-M1	
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