XC-5 Hardware Manual

Version 1.1

XMOS

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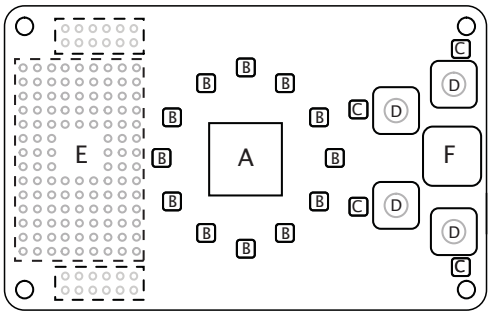
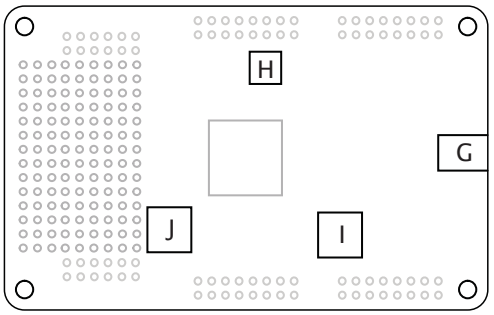
1 Introduction

The XC-5 is an event-driven processor development board based on the XMOS XS1-L1 programmable device. It comprises a single-core XS1-L1 64LQFP device, 16 user-configurable LEDs, four push-button switches, a speaker, SPI flash, JTAG and serial interfaces, and a through-hole prototyping area for connecting external components. The XC-5 is powered directly from a host PC using a mini-USB cable.

The diagram below shows the layout of the main components on the card:





A XS1-L1 Device

B Twelve Red/Green User LEDs

C Four Green User LEDs

D Four Push-Button Switches

E Prototyping Area

F Speaker

G Mini USB-B Connector

H 20MHz Crystal Oscillator

I USB 2.0 to JTAG

J SPI Flash

The XC-5 Development Kit includes a USB cable for powering and booting the device from a PC. The card is fitted with four detachable plastic feet.

The following sections in this document provide a detailed description of these components.

2 XS1-L1 Device [A]

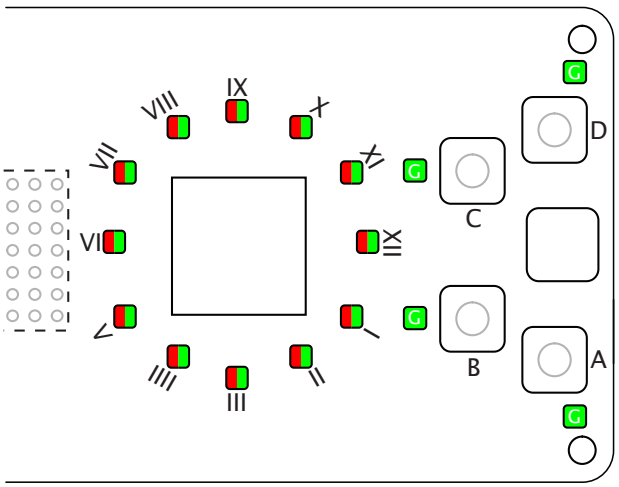
The XC-5 provides a single core XS1-L1 device in a 64LQFP package. The XCore is programmable and comprises an event-driven multi-threaded processor with tightly integrated general purpose I/O pins and 64 KBytes of on-chip RAM. The pins on the XCore are brought out of the package and connected to the card's components as follows:

- Twelve red/green and four green LEDs
- Four push-button switches
- Speaker

The processor has ports that are directly connected to the I/O pins. Examples of how to write software that interfaces over these ports with the XC-5 components is provided in a separate tutorial [1].

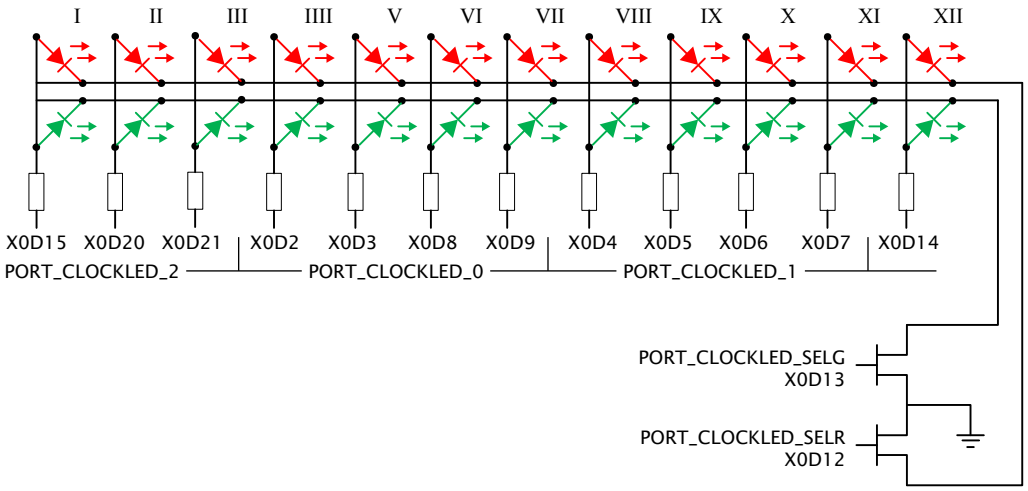
3 User-configurable LEDs [B and C]

The XC-5 has 16 user-configurable LEDs. Four of green LEDs are positioned next to the four push-buttons (collectively referred to as button-LEDs) and contain green diodes. The other 12 LEDs are positioned around the XS1-L1 in a circle (collectively referred to as clock-LEDs) and contain red/green diodes. A Roman numeral is printed next to each LED. Each of the LEDs can be driven by software. The layout of the LEDs is shown below.



To reduce the number of pins required for the 12 clock-LEDs, the LED anodes are connected to three 4-bit ports (4A, 4B and 4C) and the cathodes are connected to two 1-bit ports (1E for red, 1F for green) that are active high.

The schematic for the clock-LEDs is shown below



PORT_CLOCKLED_SELR	PORT_CLOCKLED_SELG	Colour
0	0	Off
0	1	Green
1	0	Red
1	1	Red
To get yellow, alternate green/red in 4:1 ratio		

The clock LED pins are mapped to ports as described in the table on the following page:

Pin	Port		Processor
	1b	4b	0
XD2		P4A0	PORT_CLOCKLED_0 [IIII]
XD3		P4A1	PORT_CLOCKLED_0 [V]
XD4		P4B0	PORT_CLOCKLED_1 [VIII]
XD5		P4B1	PORT_CLOCKLED_1 [IX]
XD6		P4B2	PORT_CLOCKLED_1 [X]
XD7		P4B3	PORT_CLOCKLED_1 [XI]
XD8		P4A2	PORT_CLOCKLED_0 [VI]
XD9		P4A3	PORT_CLOCKLED_0 [VII]
XD12	P1E0		PORT_CLOCKLED_SELR
XD13	P1F0		PORT_CLOCKLED_SELG
XD14		P4C0	PORT_CLOCKLED_2 [XII]
XD15		P4C1	PORT_CLOCKLED_2 [I]
XD20		P4C2	PORT_CLOCKLED_2 [II]
XD21		P4C3	PORT_CLOCKLED_2 [III]

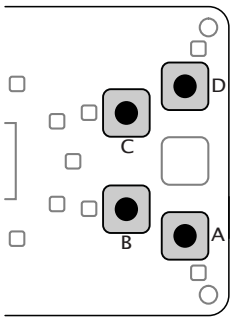
The button LED pins are mapped to ports as described in the table below:

Pin	Port	Processor
	4b	0
XD26	P4E0	PORT_BUTTONLED [A]
XD27	P4E1	PORT_BUTTONLED [D]
XD32	P4E2	PORT_BUTTONLED [C]
XD33	P4E3	PORT_BUTTONLED [B]

NOTE: The pins attached to the push-button LEDs are mapped to PORT_4E in a different bit order to the pins attached to the push-button switches and PORT_4D.

4 Push-Button Switches [D]

The XC-5 provides four push-button switches whose states can be sampled at any time by software. Pushing a button results in a 0 signal, unpushed the signal is 1. The layout of the push-buttons is shown below.



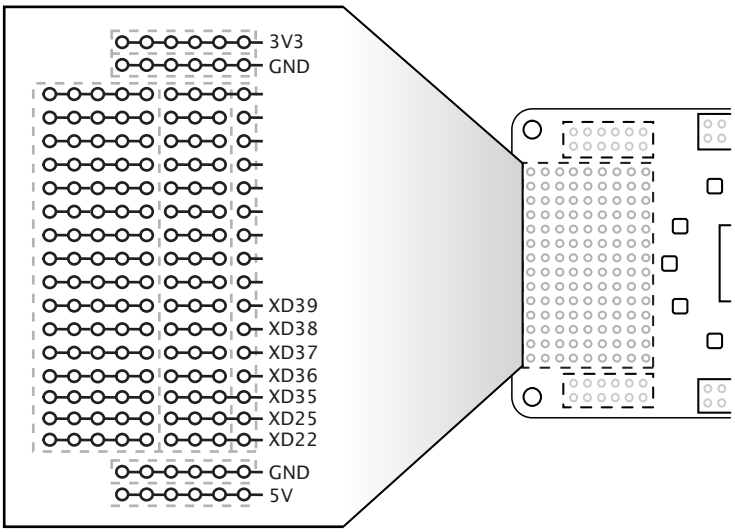
The push buttons are connected to four pins, which are mapped to ports as described in the table below.

Pin	Port	Processor
	4b	0
XD16	P4D0	PORT_BUTTON [A]
XD17	P4D1	PORT_BUTTON [B]
XD18	P4D2	PORT_BUTTON [C]
XD19	P4D3	PORT_BUTTON [D]

5 Prototyping Area [E]

The XC-5 provides a 0.1" pitch plated through hole area for adding components to the card.

The routing of I/O and power pins in the prototyping area is shown below.

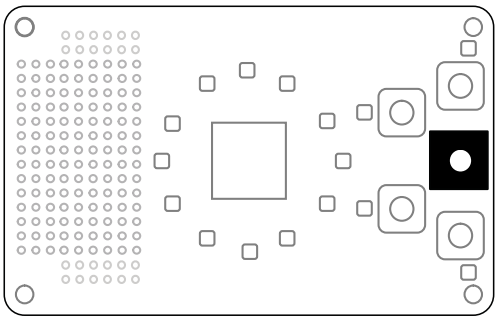


The prototyping area provides a bank of 7 I/O pins, which are mapped to 1-bit ports on the processor as described in the table below.

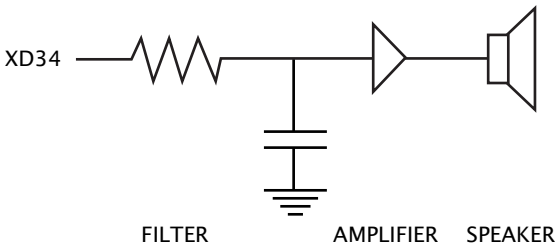
Pin	Port	Processor
	1b	
XD22	P1G0	PROTOTYPE_AREA_0
XD25	P1J0	PROTOTYPE_AREA_1
XD35	P1L0	PROTOTYPE_AREA_2
XD36	P1M0	PROTOTYPE_AREA_3
XD37	P1N0	PROTOTYPE_AREA_4
XD38	P1O0	PROTOTYPE_AREA_5
XD39	P1P0	PROTOTYPE_AREA_6

6 Speaker [F]

The XC-5 has a speaker. The layout of the speaker is shown below



Audio signals are generated by filtering pulse width modulated (PWM) digital signals to form an analogue waveform, which is amplified and sent to the speaker, as shown below:



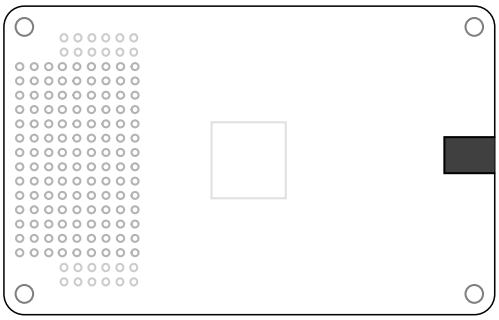
The speaker pin is mapped to a port, as shown in the table below:

Pin	Port	Processor
	1b	0
XD34	P1K0	PORT_SPEAKER

7 USB Connector [G and I]

The XC-5 is powered directly from a host PC using a USB connector. The 5V voltage is converted by the on-board regulator to the 1V and 3V3 supplies used by the components.

The USB connector can also be used to load and debug code on the XS1-L1 processor. The USB connector provides JTAG control, system reset, processor debug, and two UART links. The layout of the USB connector is shown below.



On power on, the XS1-L1 boots from the on-board flash memory. The XS1-L1 can then be put into JTAG mode by the PC, which then boots another program.

Two UART pins are mapped to ports, as shown in the table below.

Pin	Port	Processor
	1b	0
XD23	P1H0	PORT_UART_TX [XS1 to HOST]
XD24	P1I0	PORT_UART_RX [HOST TO XS1]

A UART can be implemented in software by sampling and driving these ports at the required rate. The connector performs a UART-to-USB conversion on these pins, presenting a virtual COM port to the PC that can be interfaced via a terminal emulator.

8 SPI Flash Memory [J]

The XC-5 provides 4Mbit of Serial Peripheral Interface (SPI) flash memory, which is interfaced by the four 1-bit connections described in the table on page 13.

Pin	Port	Processor
	1b	0
XD0	P1A0	PORT_SPI_MISO
XD1	P1B0	PORT_SPI_SS
XD10	P1C0	PORT_SPI_CLK
XD11	P1D0	PORT_SPI_MOSI

The include the XFLASH utility for programming compiled programs into the flash memory. XC-5 designs may also access the flash memory at run-time by interfacing with the above ports.

9 20MHz Crystal Oscillator [H]

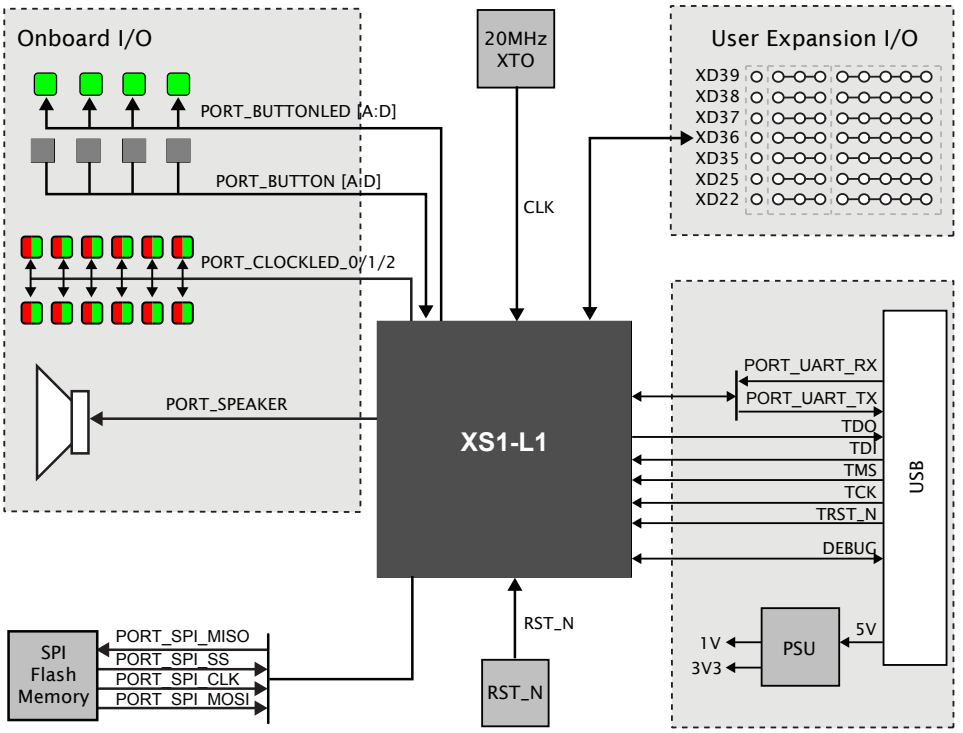
The XS1-L1 is clocked at 20MHz by a crystal oscillator on the card. The processor is clocked at 400MHz, the I/O ports at 100MHz, by an on-chip phase-locked loop (PLL).

10 Dimensions

The XC-5 dimensions are 86 x 54mm. The mounting holes are 3mm in diameter.

11 XC-5 Block Diagram

The diagram below shows how the XC-5 components are connected to the XS1-L1.



11.1 I/O Port-to-Pin Mapping

The table below provides a full description of the port-to-pin mappings described throughout this document.

Pin	Port				Processor
	1b	4b	8b	16b	
XD0	P1A0				PORT_SPI_MISO
XD1	P1B0				PORT_SPI_SS
XD2		P4A0	P8A0	P16A0	PORT_CLOCKLED_0 [IIII]
XD3		P4A1	P8A1	P16A1	PORT_CLOCKLED_0 [V]
XD4		P4B0	P8A2	P16A2	PORT_CLOCKLED_1 [VIII]
XD5		P4B1	P8A3	P16A3	PORT_CLOCKLED_1 [IX]
XD6		P4B2	P8A4	P16A4	PORT_CLOCKLED_1 [X]
XD7		P4B3	P8A5	P16A5	PORT_CLOCKLED_1 [XI]
XD8		P4A2	P8A6	P16A6	PORT_CLOCKLED_0 [VI]
XD9		P4A3	P8A7	P16A7	PORT_CLOCKLED_0 [VII]
XD10	P1C0				PORT_SPI_CLK
XD11	P1D0				PORT_SPI_MOSI
XD12	P1E0				PORT_CLOCKLED_SELR
XD13	P1F0				PORT_CLOCKLED_SELG
XD14		P4C0	P8B0	P16A8	PORT_CLOCKLED_2 [XII]
XD15		P4C1	P8B1	P16A9	PORT_CLOCKLED_2 [I]
XD16		P4D0	P8B2	P16A10	PORT_BUTTON [A]
XD17		P4D1	P8B3	P16A11	PORT_BUTTON [D]
XD18		P4D2	P8B4	P16A12	PORT_BUTTON [C]
XD19		P4D3	P8B5	P16A13	PORT_BUTTON [B]
XD20		P4C2	P8B6	P16A14	PORT_CLOCKLED_2 [II]
XD21		P4C3	P8B7	P16A15	PORT_CLOCKLED_2 [III]
XD22	P1G0				PROTOTYPE_AREA_0
XD23	P1H0				PORT_UART_TX [XS1 TO HOST]
XD24	P1I0				PORT_UART_RX [HOST TO XS1]
XD25	P1J0				PROTOTYPE_AREA_1
XD26		P4E0			PORT_BUTTONLED [A]
XD27		P4E1			PORT_BUTTONLED [B]
XD32		P4E2			PORT_BUTTONLED [C]
XD33		P4E3			PORT_BUTTONLED [D]
XD34	P1K0				PORT_SPEAKER
XD35	P1L0				PROTOTYPE_AREA_2
XD36	P1M0				PROTOTYPE_AREA_3
XD37	P1N0				PROTOTYPE_AREA_4
XD38	P1O0				PROTOTYPE_AREA_5
XD39	P1P0				PROTOTYPE_AREA_6

12 XC-5 XN File

The XCore pins linked to the XC-5 hardware features are mapped to generic port identifiers in the platform specific XN file, to simplify the process of porting a project between platforms.

The following table lists the defined port identifiers:

Port Location	Generic Identifier
XS1_PORT_1A	PORT_SPI_MISO
XS1_PORT_1B	PORT_SPI_SS
XS1_PORT_1C	PORT_SPI_CLK
XS1_PORT_1D	PORT_SPI_MOSI
XS1_PORT_4A	PORT_CLOCKLED_0
XS1_PORT_4B	PORT_CLOCKLED_1
XS1_PORT_4C	PORT_CLOCKLED_2
XS1_PORT_1E	PORT_CLOCKLED_SELR
XS1_PORT_1F	PORT_CLOCKLED_SELG
XS1_PORT_4D	PORT_BUTTON
XS1_PORT_4E	PORT_BUTTONLED
XS1_PORT_1H	PORT_UART_TX
XS1_PORT_1I	PORT_UART_RX
XS1_PORT_1K	PORT_SPEAKER

13 Related Documents

The following documents provide more information on designing with the XC-5:

- *XCard-5 Tutorial* [1]: provides an introduction to programming software on the XC-5 using the XC language.
- *XCore XS1 Architecture Tutorial* [2]: provides an overview of the XS1 instruction set architecture.

The most up-to-date information on the XC-5, including board schematics and product datasheets, is available from:

- `http://www.xmos.com/xc5/`

Bibliography

[1] XMOS Ltd. XC-5 Development Card Tutorial. Website, 2009. http://www.xmos.com/published/xc5tut.

[2] David May and Henk Muller. XCore XS1 Architecture Tutorial. Website, 2009. http://www.xmos.com/published/xs1tut.

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